GX2711 1.6 TO 3.2 GBPS TRANSCEIVER

FEATURES

- 1.6 to 3.2 Gigabits Per Second (Gbps) Serializer /Deserializer
- Hot-Plug Protection
- Low Power Operation
- Programmable Pre emphasis Levels on Serial Output
- Interfaces to Backplane, Copper Cables, or Optical Converters
- On chip 8-bit/10-bit Encoding/Decoding, Comma Detect
- On-Chip PLL Provides Clock Syn-thesis from Low-Speed Reference
- Low Power: 290 mW
- 3 V Tolerance on Parallel Data Input Signals
- 16-Bit Parallel TTL Compatible Data Interface
- Loss of Signal (LOS) Detection
- Integrated 50-Ω Termination Resistors on RX
- QFN60 package

APPLICATIONS

- Point-to-point high-speed I/O
- Data acquisition
- Data processing

Version: V1.6
Released Date: 2024/03/07

FUNCTIONAL BLOCK DIAGRAM

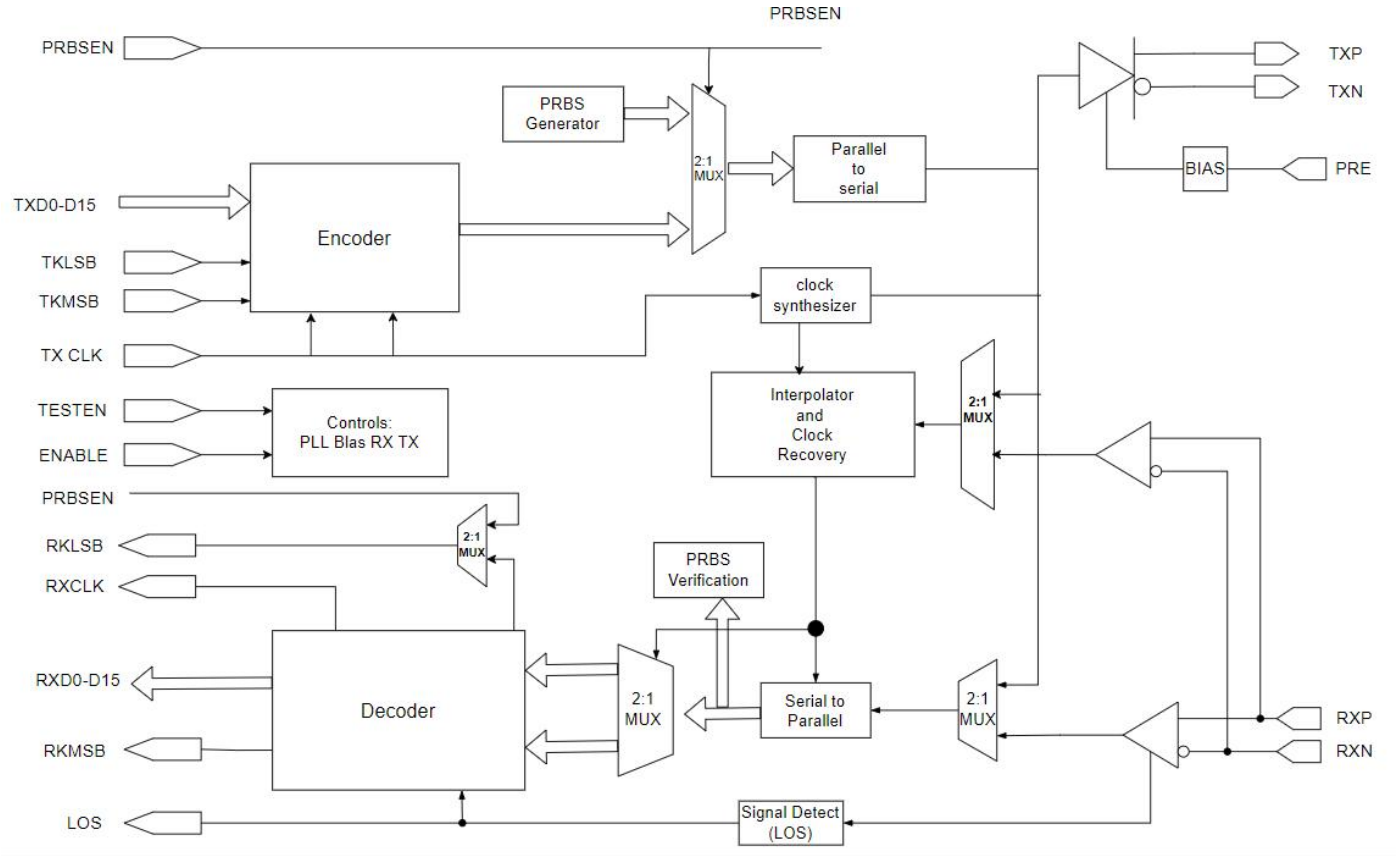


Figure 1. GX2711 Block Diagram

TABLE OF CONTENTS

DESCRIPTION

GX2711 is used for ultra high-speed bidirectional point-to-point data transmission systems. GX2711 supports effective serial interface speeds of 1.6 Gbps to 3.2 Gbps, providing data bandwidth of up to 3.2 Gbps.

GX2711 is the ideal choice for high-speed backplane interconnection and point-to-point data links.

The following sections introduce the block characteristics and operation methods of each module of the GX2711 transceiver.

Transmit interface

The transmitter portion registers valid incoming 16-bit wide data (TXD [0:15]) on the rising edge of the TXCLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (TXCLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (TXD0) first.

Transmit data bus

The transmit bus interface accepts 16-bit single-ended TTL parallel data at the TXD[0:15] terminals. Data and comma control is valid on the rising edge of the TXCLK. The TXCLK is used as the word clock. The data, comma, and clock signals must be properly aligned as shown in Figure 2.

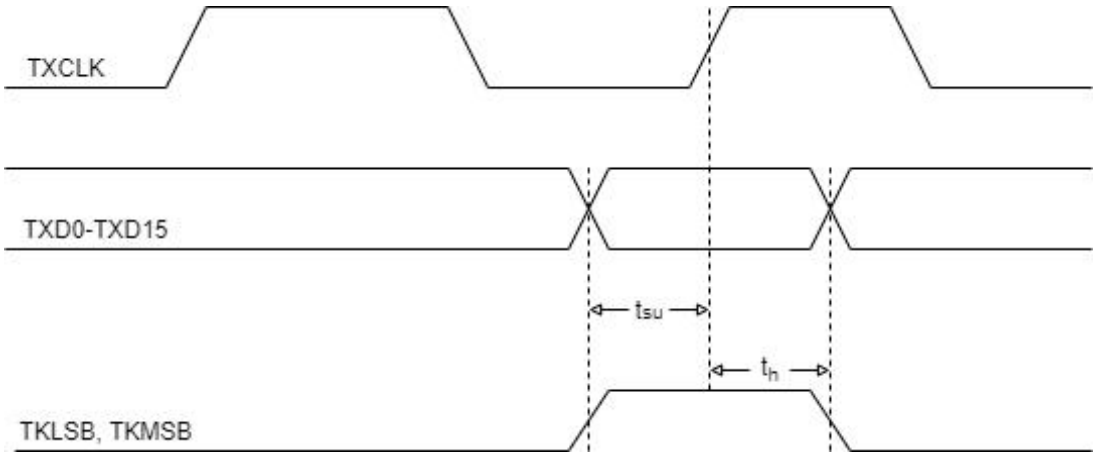


Figure 2. Transmit Timing Waveform

Transmission latency

The data transmission latency of the GX2711 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum transmit latency $t_{d(Tx\ latency)}$ is 34 bit times; the maximum is 38 bit times. Figure 3 illustrates the timing relationship between the transmit data bus, the TXCLK, and the serial transmit terminals.

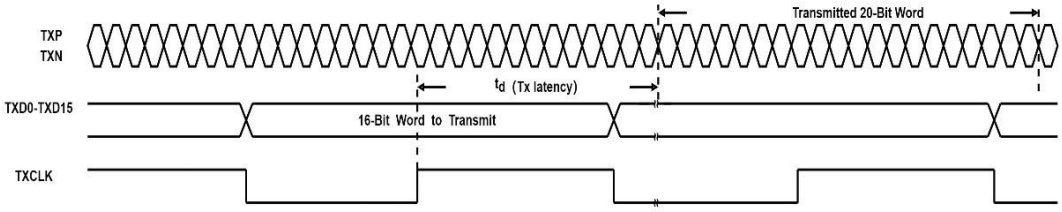


Figure 3. Transmitter Latency

8-bit/10-bit encoder

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The GX2711 uses the 8-bit/10-bit encoding algorithm that is used by fibre channel and gigabit ethernet. This is transparent to the user, as the GX2711 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. Since the GX2711 is a 16-bit wide interface, the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependent upon two additional input signals, the TKMSB and TKLSB.

Table 1. Transmit Data Controls

TKLSB	TKMSB	16 BIT PARALLEL INPUT	
0	0	Valid data on TXD (0–7)	Valid data on TXD (8–15)
0	1	Valid data on TXD (0–7)	K code on TXD (8–15)
1	0	K code on TXD (0–7)	Valid data on TXD (8–15)

1	1	K code on TXD (0–7)	K code on TXD (8–15)

PRBS generator

The GX2711 has a built-in 27-1 PRBS (pseudorandom bit stream) function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode.

The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another GX2711, or looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

Parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the TXCLK input frequency. The LSB (TXD0) is transmitted first.

High-speed data output

The high-speed data output driver consists of a voltage mode logic (VML) differential pair optimized for a 50-Ω impedance environment. The magnitude of the differential pair signal swing is compatible with pseudo emitter coupled logic (PECL) levels when ac-coupled.

The line can be directly-coupled or ac-coupled. The outputs also provide preemphasis to compensate for ac loss when driving a cable or PCB backplane trace over a long distance (see Figure 4). The level of preemphasis is controlled by PRE as shown in Table 2 .

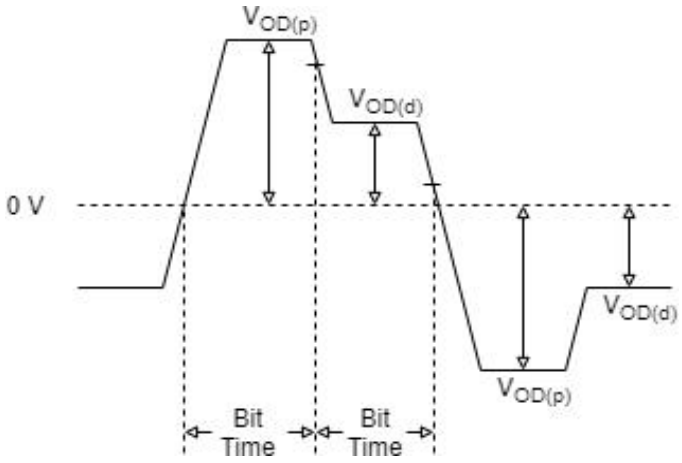


Figure 4. Output Voltage Under Pre-emphasis (|VTXP–VTXN|)

Table 2. Programmable Pre-emphasis

PRE	PREEMPHASIS LEVEL(%) $V_{OD(P)}$,$V_{OD(D)}$
0	5%
1	20%

Receive interface

The receiver portion of the GX2711 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit locks to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream.

The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10- bit decoded and output on a 16-bit wide parallel bus synchronized to the extracted receive clock. The data is received LSB (RXD0) first.

Receive data bus

The receive bus interface drives 16-bit wide single-ended TTL parallel data at the RXD [0:15] terminals. Data is valid on the rising edge of the RXCLK. The RXCLK is used as the recovered word clock.

The data, RKLSB, RKMSB, and clock signals are aligned as shown in Figure 5. Detailed timing information can be found in the switching characteristics table.

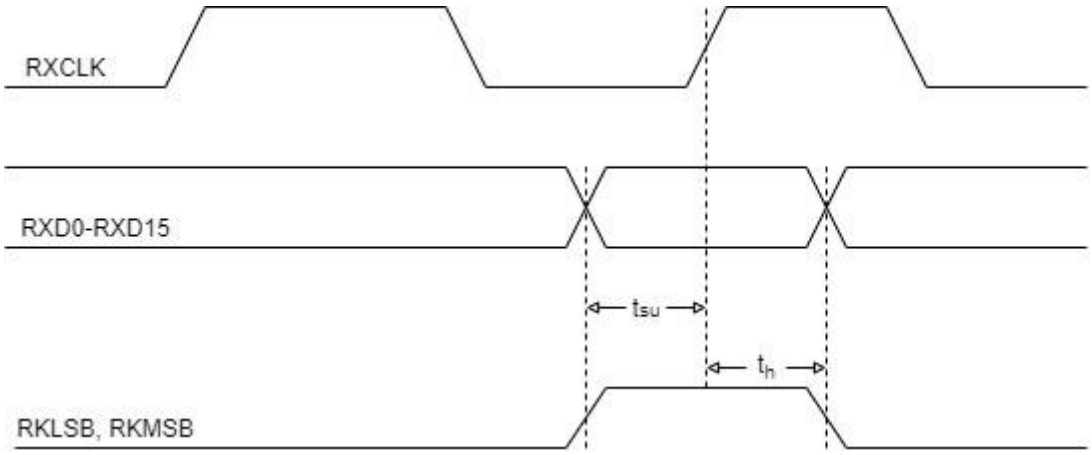


Figure 5. Receive Timing Waveform

Data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum receive latency $t_{d(Rx\ latency)}$ is 76 bit times; the maximum is 107 bit times. Figure 6 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RXCLK), and the receive data bus.

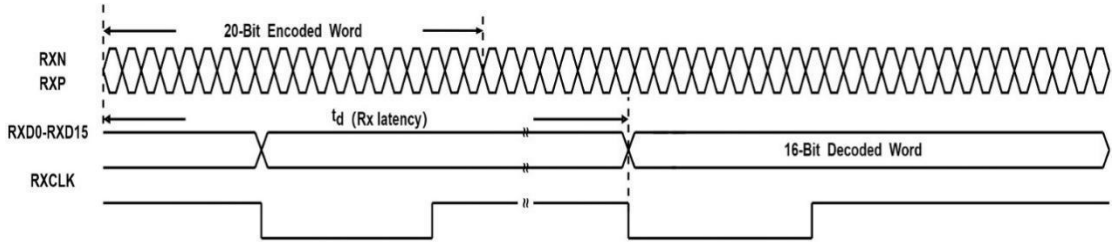


Figure 6. Receiver Latency

Serial-to-parallel

Serial data is received on the RXP and RXN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then fed into the serial to parallel converter and aligned with the word boundaries of the two decoders by detecting the Comma, thereby sending the 10-bit parallel data to each of the two 8B/10B decoders.

Comma detect and 8-bit/10-bit decoding

The GX2711 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10 bit encoded data (half of the 20-bit received word) back into 8 bits. The comma detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code.

When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. Generally this is accomplished through the use of a synchronization pattern.

This is generally a unique pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma detect circuit on the GX2711 to align the received serial data back to its original byte boundary.

The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RXCLK) and output valid on the rising edge of the RXCLK.

Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted , an 8-bit/10-bit comma was received and the specific comma is presented on the data bits RXD0–RXD7; otherwise, an 8-bit/10-bit D code was received. When RKMSB is asserted, an 8-bit/10-bit comma was received and the specific comma is presented on data bits RXD8–RXD15; otherwise, an 8-bit/10-bit D code was received (see Table 3). The valid comma the GX2711 decodes are provided in Table 4. An error detected on either byte, including comma not in Table 4, causes that byte only to indicate a K0.0 code on the RK×SB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal causes a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit

code.

Table 3. Receive Status Signals

RKLSB	RKMSB	DECODED 20 BIT OUTPUT	
0	0	Valid data on RXD (0–7)	Valid data RXD (8–15)
0	1	Valid data on RXD (0–7)	K code on RXD (8–15)

1	0	K code on RXD (0–7)	Valid data RXD (8–15)
1	1	K code on RXD (0–7),	K code on RXD (8–15)

Table 4. Valid K Characters

K CHARACTER	RECEIVE DATA BUS RXD7:RXD0 OR RXD15:RXD8
K28.0	000 11100
K28.1	001 11100
K28.2	010 11100
K28.3	011 11100
K28.4	100 11100
K28.5	101 11100
K28.6	110 11100
K28.7	111 11100
K23.7	111 10111
K27.7	111 11011
K29.7	111 11101
K30.7	111 11110

Loss of signal detection

The GX2711 has a LOS detection circuit to indicate that the input signal no longer has enough amplitude to keep the clock recovery circuit locked. The signal detection circuit aims to roughly reflect the situation of signal error, such as unplugging the cable or no signal being transmitted, without indicating whether the signal encoding is normal. In LOS mode, the RKLSB, RKMSB, and RXD0 to RXD15 pins of GX2711 are pulled up. As long as the differential amplitude of the differential signal exceeds 200mV, the LOS circuit will not generate an error signal. When the device is disabled (ENABLE=L), RKMSB will output the status of LOS. Low level valid indicates detection of LOS.

PRBS verification

The GX2711 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the RKLSB terminal low.

Reference clock input

The reference clock (TXCLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency-locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the reference clock.

Operating frequency range

The GX2711 can operate at a serial data rate from 1.6 Gbps to 3.2 Gbps. To achieve these serial rates, TXCLK must be within 80 MHz to 160 MHz. The TXCLK must be within ±100 PPM of the desired parallel data rate clock.

Testability

The GX2711 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for BIST (built-in self-test).

Built-in self-test (BIST)

The GX2711 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RKLSB terminal.

Power-on reset

The GX2711 power-on reset process is as follows:

1. Keep GX2711 to steady power-on state. during the power-on, make sure that ENABLE, LCKREFEN is logic high, PRBSEN is logic low.
2. Establish the clock GTX_CLK.
3. Set ENABLE to logic high and wait for 200us.

4. (a) On the falling edge of clock GTX_CLK, TKLSB is set to logic high and TXD<7:0> is set to 0xBC, while TKMSB is set to logic low and there is no limit on TXD<15:8>and waits for 100us.

   (b) After setting TKLSB logic high, waiting 20us.

   (c) Set LCKREFEN logic low , waits for 20us then set LCKREFEN logic high.

5. TKLSB and TKMSB are set low and then TXD<15:0> starts to transmit data.

Note: TKLSB/TKMSB / TXD<15:0> toggles on the falling edge of clock GTX_CLK.

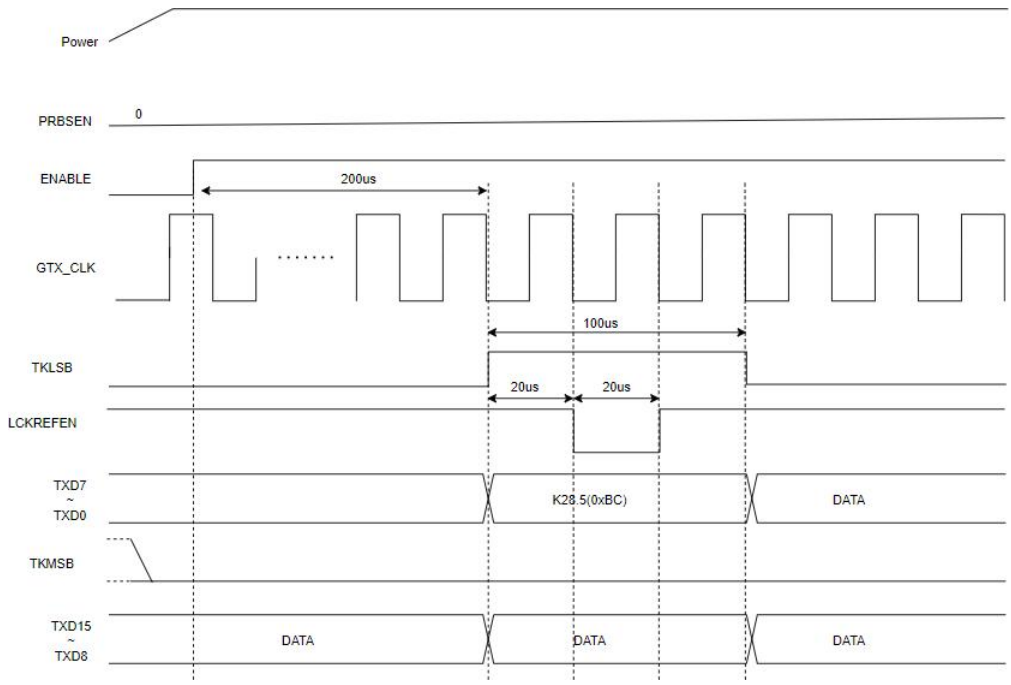


Figure 7. Power-on Reset Timing Diagram

Electrical characteristics over recommended operating conditions

Table 5. Electrical Characteristics over Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage,V_{DD}			2.5		V
Supply current, I_{CC}	1.6Gbps,PRBS pattern		100		mA
	3.2Gbps,PRBS pattern		115		
Power dissipation, P_D	1.6Gbps,PRBS pattern		250		mW
	3.2Gbps,PRBS pattern		290		mW
Shutdown current	Enable=0, V_{DDA}, V_{DD} terminals+V_{DD}=MAX		4		mA
Opterating temperature		-40		85	℃

TTL input electrical characteristics

Unless otherwise noted, TTL signals: TXDO–TXD15, TXCLK, LCKREFN, ENABLE, PRBS_EN, TKLSB, TKMSB, PRE.

Table 6. Input Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	See figure 8		2.5	3.6	V
Low-level input voltage, V_{IL}	See figure 8			0.8	V
Input high current, I_{IH}	V_{DD}=MAX, V_{IN}=2V			40	μA
Input low current, I_{IL}	V_{DD} =MAX, V_{IN} = 0.4 V	-40			μA
C_I		4			pF
t_r	0.7 to 1.9 V, C = 5 pF, See figure 8	1			ns
t_f	1.9 to 0.7 V, C = 5 pF, See figure 8	1			ns
t_{su}	See figure 8	1.5			ns
t_h	See figure 8	1.5			ns

transmitter/receiver characteristics

Table 7. transmitter/receiver characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Differential output peak-to-peak voltage, $V_{OD(pp)}$	See figure 10		2400		mVp-p

Deemphais output voltage, $V_{OD(d)}$ $V_{OD(d)}=\|V_{TXP}-V_{TXN}\|$	See figure 10，PRE=high		2100		mVp-p
Transmit common mode voltage range, $V_{(cmt)}$ $V_{(cmt)}=(V_{TxP}+V_{TxN})$ /2	See figure 10		1150		mV
Receiver input voltage differential, V_{ID} $V_{ID=}\|V_{RxP}-V_{RxN}\|$		200		1600	mV
Receiver common mode voltage range, V(cmr) V(cmr) = (VRXP+ VRXN) / 2			1150		mV
Receiver input leakage current, I_{IKG}		-10		10	μA
Receiver input capacitance, C_I				2	pF
Serial data total jitter (peak-to-peak)	Differential output jitter at 3.2Gbps, Random + deterministic, PRBS pattern		0.22		UI
	Differential output jitter at 1.6Gbps, Random + deterministic, PRBS pattern		0.15		
Differential output signal rise, fall time (20% to 80%), t_t,t_f	RL = 50 Ω, CL = 5 pF,		150		ps

Reference clock (TXCLK) timing requirements

Table 8. reference clock (TXCLK) timing requirements

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Frequency	Receiving data rate /20	-100		+100	ppm
Frequency tolerance		-100		+100	ppm
Duty cycle		40		60	%
Jitter	Peak-to-peak			40	ps

TTL output switching characteristics

Table 9. TTL output switching characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
High-level output voltage, V_{OH}	I_{OH} = –2 mA, V_{DD} = MIN	2.1	2.3		V
Low-level output voltage, V_{OL}	I_{OL} =2 mA, V_{DD} =MIN	GND	0.25	0.5	V
Slew rate (rising), magnitude of RXCLK, RKLSB, RKMSB, RXD[0..15], $t_{r(slew)}$	0.8 V to 2 V, C = 5 pF, See figure 9	0.5			V/ns
Slew rate (falling), magnitude of RXCLK, RKLSB, RKMSB, RXD[0..15], $t_{f(slew)}$	0.8 V to 2 V, C = 5 pF, See figure 9	0.5			V/ns

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
RXD[0..15] RKMSB RKLSB setup to ↑ RXCLK , t_{su}	50% voltage swing, TXCLK = 80 MHz, See figure 9	3			ns
	50% voltage swing, TXCLK = 125 MHz, See figure 9	2.5			
RXD[0..15] RKMSB RKLSB hold to ↑ RXCLK , t_h	50% voltage swing, TXCLK = 80 MHz, See figure 9	2			ns
	50% voltage swing, TXCLK = 125 MHz, See figure 9	1.5			

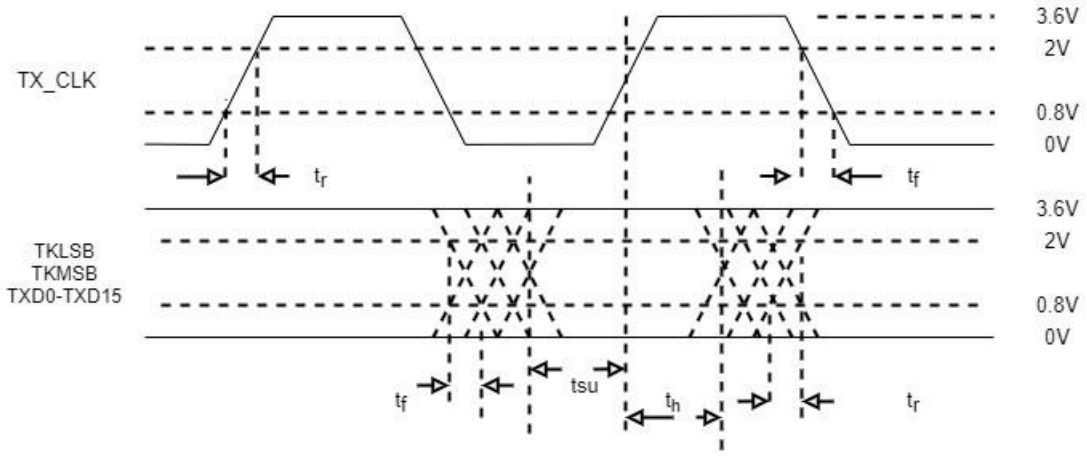


Figure 8. TTL Data Input Valid Levels for AC Measurements

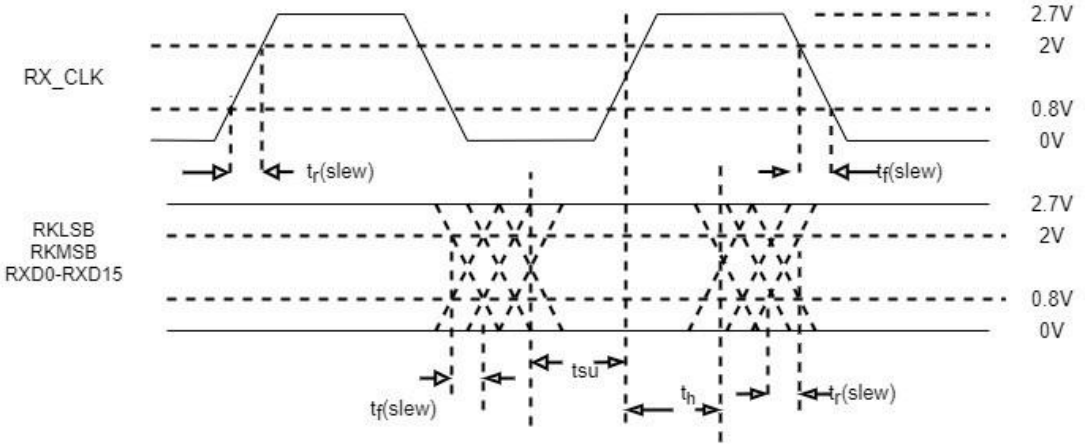


Figure 9. TTL Data Output Valid Levels for AC Measurements

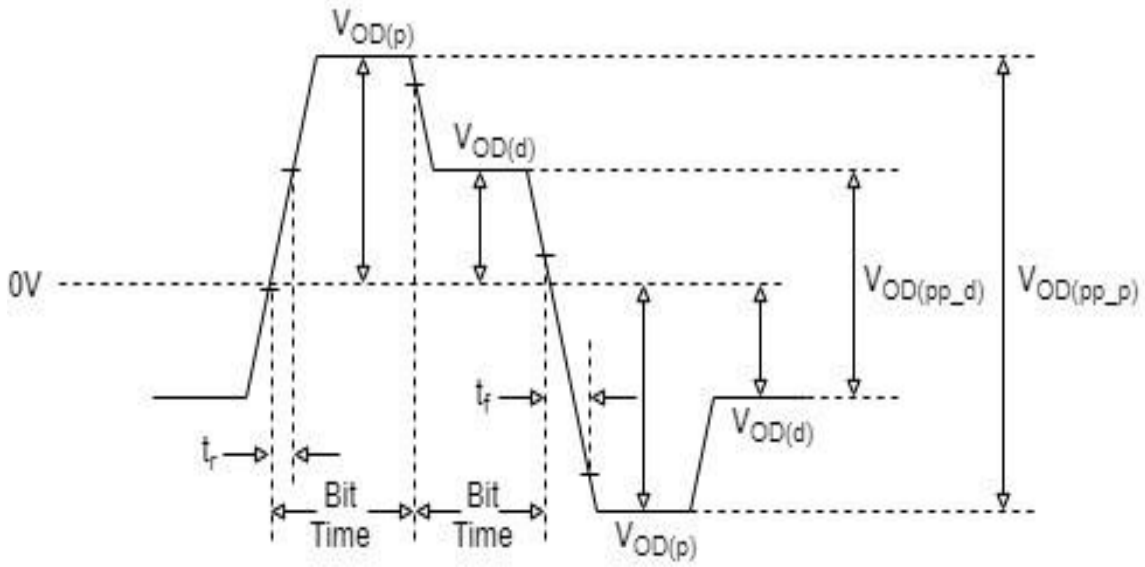


Figure 10. Differential common mode output voltage

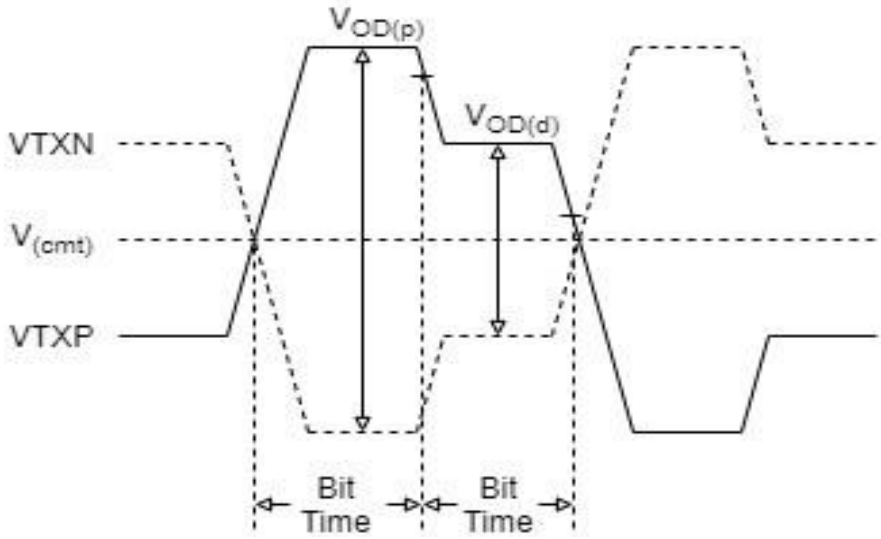


Figure 11. Definition of common mode output voltage

ABSOLUTE MAXIMUM RATINGS

VDD ……..……..……-0.3V to 3V

Voltage: TXD0-TXD15, NABLE, XCLK, KMSB, KLSB, OOPEN, RBSEN, LCKREFN, PRE, TESTEN…….……..……-0.3V to 4V

Voltage: RXD0-RXD15, RKMSB, RKLSB, RX_CLK……..……..…..……-0.3V to VDD+0.35V

Voltage: DINRXP, DINRXN, DOUTTXP, DOUTTXN……...……..…-0.35V to +VDDA+0.35V

Maximum exposure time for unpowered transceivers with external inputs……..……<10hours

ESD(HBM) …….……..……..…….3000V

ESD(CDM) ……..……..…….1500V

Operating temperature…….……..……..-40°C to 85°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Caution

This product is an electrostatic sensitive device. Therefore, proper ESD precaution measures should be taken to avoid performance degradation or loss of functionality.

PIN (PAD) CONFIGURATION AND FUNCTION DESCRIPTION

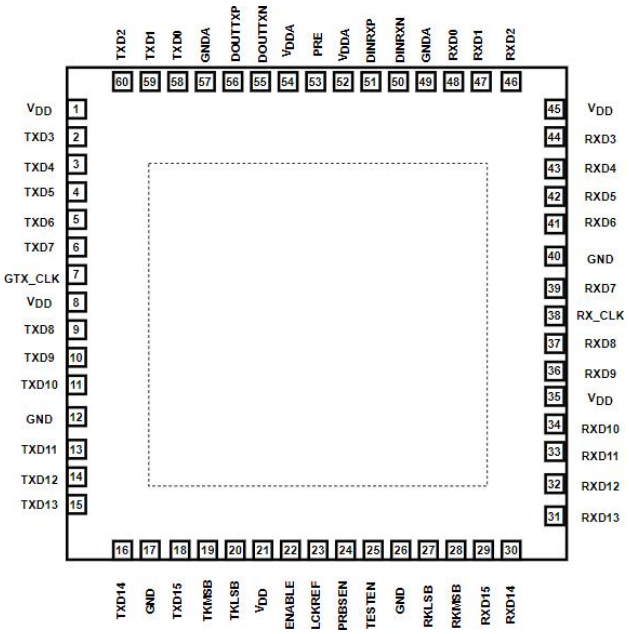


Figure 12. Pin Configuration

Table 10. Pin Definition

Pin No.	Mnemonic	I/O	Description
55 56	DOUTTXN DOUTTXP	O	Serial transmit outputs. TXP and TXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the TXCLK value.
22	ENABLE	I	Device enable. When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active and the RKMSB will output the status of the signal detection circuit (LOS). When ENABLE is set to high, the transceiver goes into power-on reset before beginning normal operation.
8,12,17,26, 40,	GND		Digital logic ground. Provides a ground for the logic circuits, digital I/O buffers and high -speed analog circuits.
49,57	GNDA		Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
23	LCKREFN	I	Lock to reference. When LCKREFN is low, the receiver clock is frequency locked to TXCLK. This places the device in a transmit only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus terminals, RXD[0:15], RXCLK and RKLSB, RKMSB are in a high-impedance state. When LCKREFN is deasserted high, the receiver is locked to the received data stream.
53	PRE	I	Pre-emphasis control. Selects the amount of pre-emphasis to be added to the high-speed

Pin No.	Mnemonic	I/O	Description
			serial output drivers. Left low or unconnected, 5% pre-emphasis is added. Pulled high, 20% pre-emphasis is added.
24	PRBSEN	I	PRBS test enable. When asserted high results of pseudo random bit stream (PRBS) tests can be monitored on the RKLSB terminal. A high on RKLSB indicates that valid PRBS is being received.
27	RKLSB	O	K-code indicator /PRBS test results. When RKLSB is asserted high, an 8-bit/10-bit K code was received and is indicated by data bits RXD0–RXD7. When RKLSB is asserted low an 8-bit/10-bit D code is received and is presented on data bits RXD0–RXD7. When PRBSEN is asserted high this pin is used to indicate status of the PRBS test results (high = pass).
28	RKMSB	O	K-code indicator. When RKMSB is asserted high an 8-bit/10-bit K code was received and is indicated by data bits RXD8 –RXD15. When RKMSB is asserted low an 8-bit/10-bit D code was received and is presented on data bits RXD8 – RXD15. If the differential signal on RXN and RXP drops below 200 mV, then RXD [0:15], RKLSB, and RKMSB are all asserted high. When the device is disabled (ENABLE=L), the RKMSB will output the status of LOS. A valid low level indicates that LOS is detected.
38	RX_CLK	O	Recovered clock. Output clock that is synchronized to RXD [0..9], RKLSB, and RKMSB. RXCLK is the recovered serial data rate clock divided by 20. RXCLK is held low during power-on reset.
29 to34, 36,37, 39,41 to 44,46 to48	RXD15 to RXD0	O	Receive data bus. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RXCLK. The data is valid on the rising edge of RXCLK as shown in Figure 5. These terminals are in high-impedance state during power-on reset.
50,51	DINRXN DINRXP	I	Serial receive inputs. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
25	TESTEN	I	Test mode enable. This terminal should be left unconnected or tied low.
20	TKLSB	I	K-code generator (LSB). When TKLSB is high, an 8-bit/10-bit K-code is transmitted as controlled by data bits TXD0 –TXD7. When TKLSB is low an 8-bit/10-bit D-code is transmitted as controlled by data bits TXD0 – TXD7.
19	TKMSB	I	K-code generator (MSB). When TKMSB is high an 8-bit/10-bit K-code is transmitted as controlled by data bits TXD8 –TXD15. When TKMSB is low an 8-bit/10-bit D-code is transmitted as controlled by data bits TXD8 – TXD15.
7	TX_CLK GTX_CLK	I	Reference clock. TXCLK is a continuous external input clock that synchronizes the transmitter interface signals TKMSB, TKLSB and TXD [0..15]. The frequency range of TXCLK is 80 MHz to 135 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data TXD [0..15] for serialization
58 to60	TXD0 to TXD2	I	Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of TXCLK as shown in Figure 2.
2 to 6,9 to 11,13 to 16,18	TXD3 to TXD15	I	

Pin No.	Mnemonic	I/O	Description
1,8,21,35,45	VDD		Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
52,54	VDDA		Analog power. VDDA provides a supply reference for the high-speed analog circuits, receiver and transmitter
0	EPAD		Ground and heat dissipation PAD

FUNCTION MODE

Shutdown Mode

When the enable pin is pulled low, the GX2711 enters off mode. In shutdown mode, the serial transmit pin (TXN), receive data bus pin (RXD0 to RXD15), and RKLSB enter a high impedance state. In off mode, the signal detection circuit consumes less than 15 mW. When the GX2711 is in off mode, a clock signal on the TXCLK pin must be provided if LOS functionality is required.

Application

The GX2711 can be applied as a bidirectional transmission function with send/receive capability, or either send only or receive only at each end of the link.

In either case, the sender is always running because a GTX_CLK is needed to provide the PLL with a reference clock. In the transmit-only case, LCKREFN can be pulled low to disable the receiver-side interface.

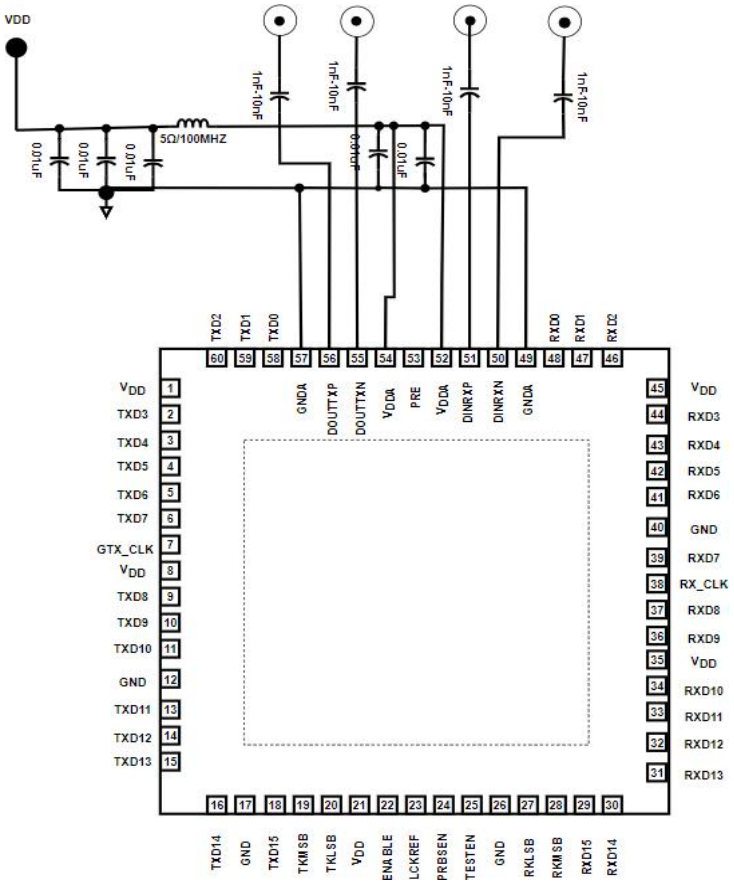


Figure 13. External Component Interconnection

High-speed I/O directly-coupled mode

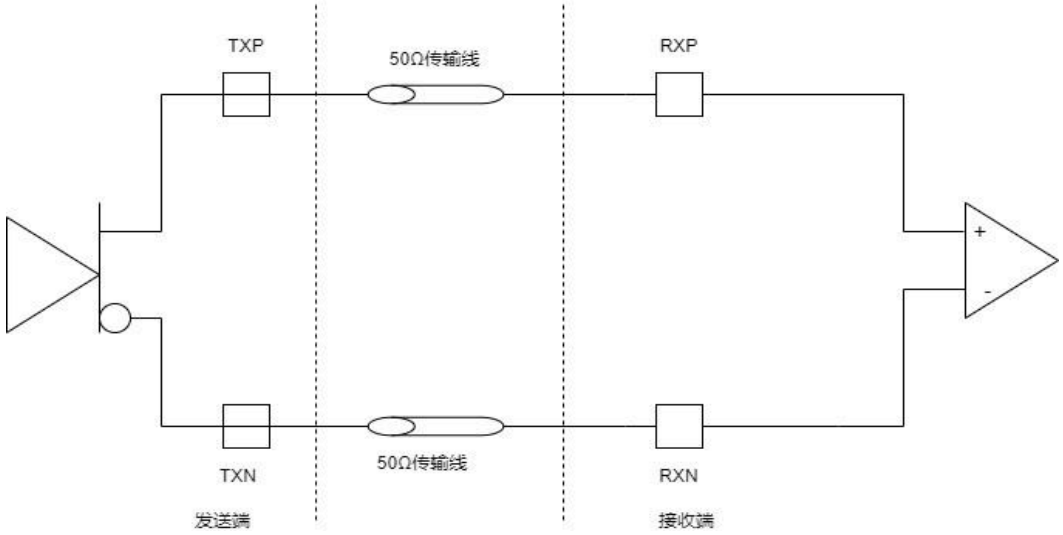


Figure 14. High-Speed I/O Directly-Coupled Mode

High-speed I/O AC-coupled mode

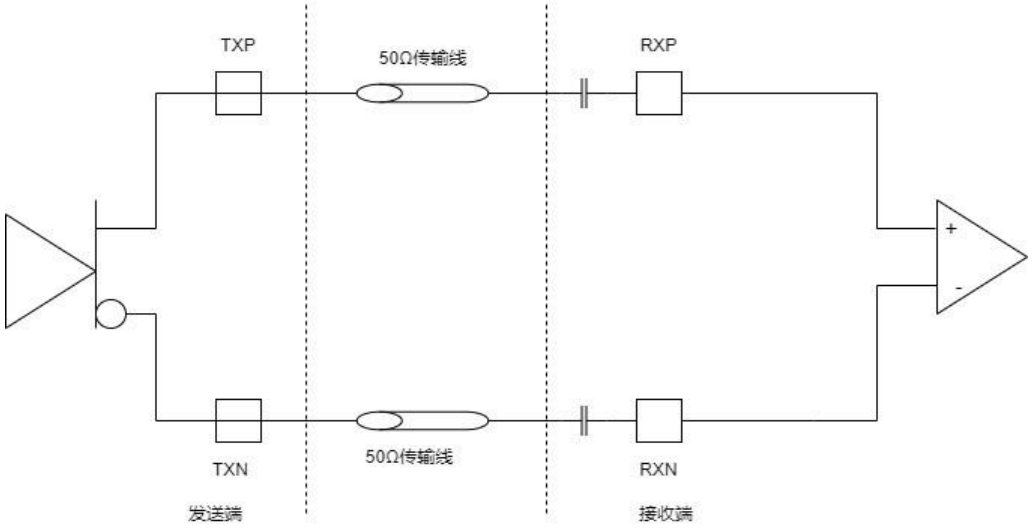


Figure 15. High-Speed I/O AC-Coupled Mode

Design requirements

The input conditions in the datasheet are established and validated based on achieving a bit error rate (BER) of 1E-12 or higher. Other aspects that affect BER include power supply noise, transmission losses, and matching of the 50Ω controlled impedance of the transmit and receive differential pins.

Detailed design process

A detailed design process involves scrutinizing system properties, design, and bit error rate targets. Understanding these attributes allows the establishment of jitter budgets to ensure that design BER goals are met.

Power requirements

The power supply must be within the recommended operating range, and power supply ripple exceeding 100mV may affect transmit jitter and receiver jitter tolerance. VDDA should be filtered out of VDD. Filter values should be set to minimize power and/or numeric logic. This numerical logic exists in a system with a range characteristic. PLL is sensitive to noise from 300 kHz to 3 MHz.

TX output eye diagram

DataRate=3.2Gbps, EW=0.8UI, EH=1.8Vdpp

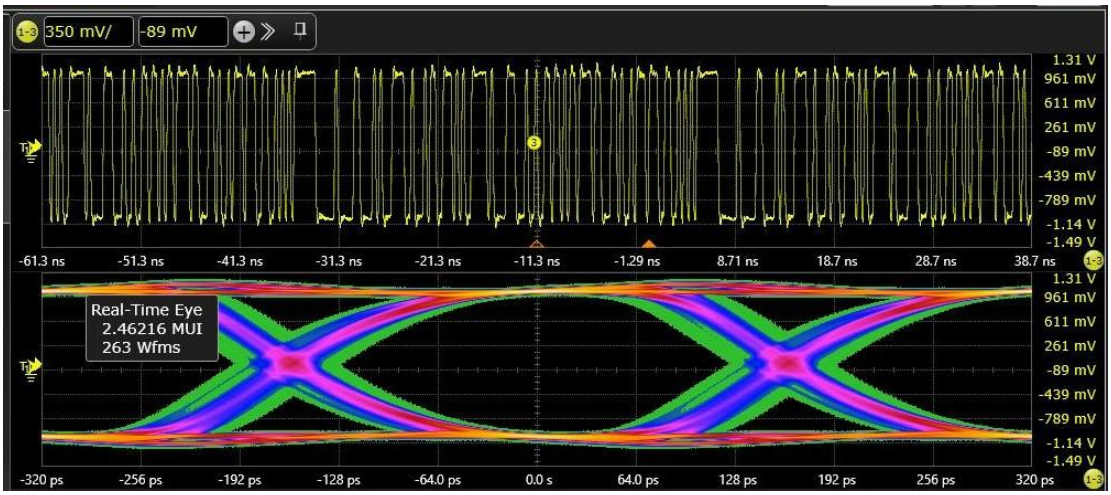
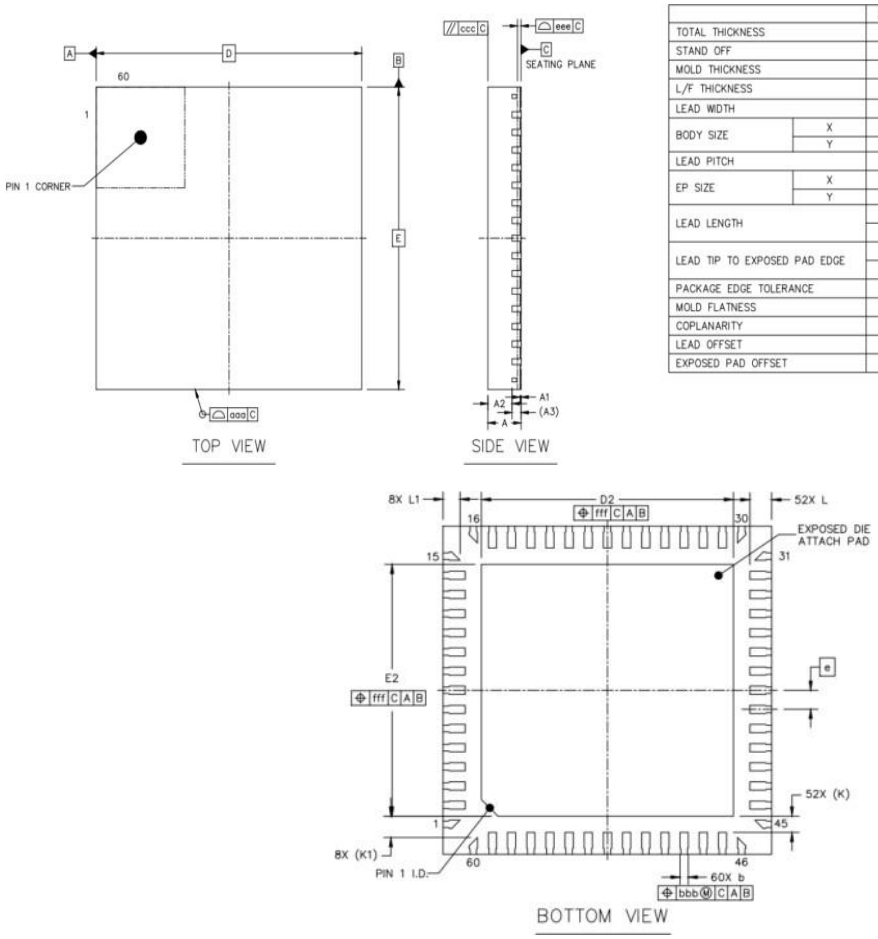


Figure 16. TX output eye diagram

OUTLINE DIMENSION



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.1	0.15	0.2
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	4.5	4.6	4.7
	Y	E2	4.5	4.6	4.7
LEAD LENGTH		L	0.3	0.4	0.5
		L1	0.207	0.307	0.407
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
		K1		0.393 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Figure 18. QFN60 (Dimension shown in mm)

ORDERING GUIDE

Table 11. Order Information

Material No.	Temperature range	Package
GX2711GDLUMY	-40°C-85°C	QFN60

Customed packages are available upon request.

DECLARATION

The information above is for reference only and is intended to assist GXSC (Shenzhen) Technology Co., Ltd customers in their design and development. GXSC (Shenzhen) Technology Co., Ltd reserves the right to change the above information without prior notice due to technological innovation.

Contact Us:
NAME：JESSE
EMAIL:service jesseli@gxschip.com
WECHAT: f40044269
FACEBOOK:GXSC
VK:@id836505054