GX1230A: 10/80SPS, 20-bit Sigma-Delta ADC with PGA

FEATURES

PGA Gain: 64 or 128
Data Rates: 10SPS or 80SPS
RMS Noise: 32nV at 10SPS
Offset Drift: 10nV/°C
Gain Drift: 2ppm/°C
Internal or External Clock
Parity Check
Power Supply
AVDD: 2.7V to 5.25V
DVDD: 2.7V to 5.25V
Current: 0.8mA Package:
16-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Pressure Sensors
Industrial Process Control

DESCRIPTION

The GX1230A is a low noise, low drift, and high-resolution 20-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) that offers high-accuracy measurement solutions for bridge sensors.

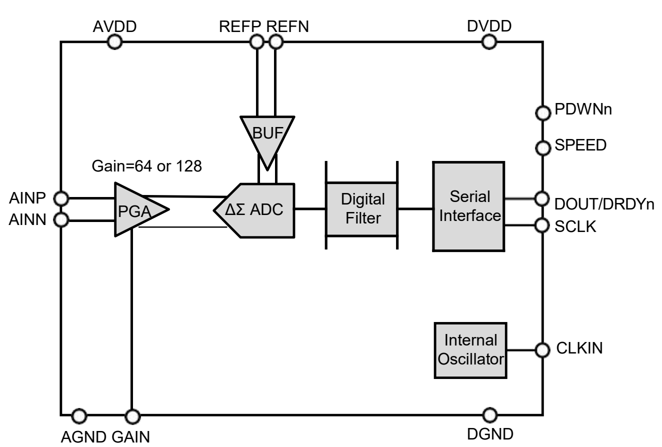
The device contains a low noise PGA with gains selected from 64 or 128, a delta-sigma (Δ-Σ) modulator, and a SINC4 digital filter. Two data rates are provided from the device: 10SPS and 80SPS.

SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

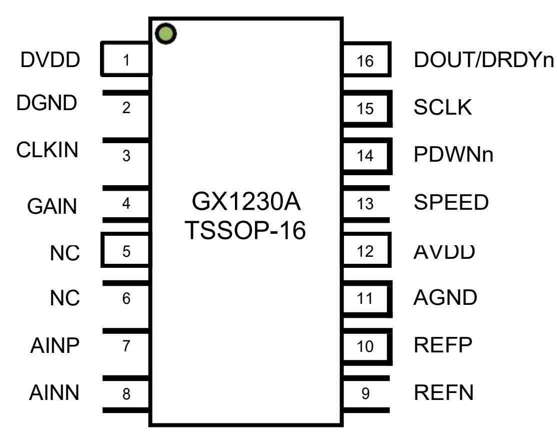
The on-chip oscillator or an external clock can be used as the clock source to the device.

The GX1230A is available in 16-lead TSSOP package and is fully specified over the -40°C to +125°C temperature range.

Function Block Diagram

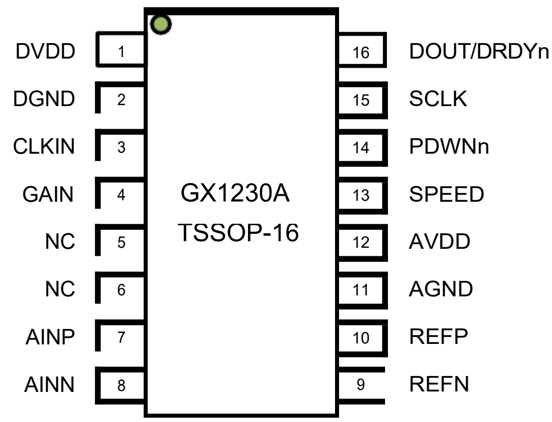


TSSOP-16



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



		FUNCTION	DESCRIPTION
1	DVDD	Digital	Digital power supply, 2.7V to 5.25V.
2	DGND	Digital	Digital ground reference point.
3	CLKIN	Digital Input	1) Internal oscillator: Connect to DGND. 2) External clock: Connect to external clock input.
4	GAIN	Digital Input	PGA gain control: DGND for gain=64 and DVDD for gain=128. Gain=64 if float.
5	NC	Digital	No connection (float) or connect to DVDD/DGND.
6	NC	Digital	No connection (float) or connect to DVDD/DGND.
7	AINP	Analog Input	Positive analog input.
8	AINN	Analog Input	Negative analog input.
9	REFN	Analog Input	Negative reference input.
10	REFP	Analog Input	Positive reference input.
11	AVSS	Analog	Negative analog power supply.
12	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to AVSS.
13	SPEED	Digital Input	Date rate select: DGND for 10SPS and DVDD for 80SPS.
14	PDWNn	Digital Input	Power-Down signal. Active low. ADC enters power-down mode if holding pin low.
15	SCLK	Digital Input	Serial data clock.
16	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
GX1230A	TSSOP-16	-40°C to +125°C	GX1230A-ITSP16-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	–0.3	6.5	V
	AVSS to DGND	–0.3	0.3	V
	DVDD to DGND	–0.3	6.5	V
	Analog input	V_{AVSS} – 0.3	V_{AVDD} + 0.3	V
	Digital input	V_{DGND} – 0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V

This integrated circuit can be damaged by ESD. GXSC recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{AVSS}=0V, V_{DVDD}=3.3V, V_{REF}=5V, f_{CLK}=1.536MHz, data rate=10SPS, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–0.5·V_{REF}$/Gain		$+0.5·V_{REF}$/Gain	V
Absolute Input Voltage		V_{AVSS} + 0.5		V_{AVDD} – 0.5	V
Common Mode Input Range		V_{AVSS} + 0.5 + $\|V_{INMAX}\|$·Gain		V_{AVDD} – 0.5 – $\|V_{INMAX}\|$·Gain	V
Absolute Input Current			±1		nA
SYSTEM PERFORMANCE					
PGA Gain			64/128		V/V
Resolution			20		Bits
Data Rate			10/80		SPS
Noise		See Noise Table 1			
Integral Nonlinearity (INL)			±15		ppm
Offset Error			±2		μV
Offset Drift vs. Temperature			±10		nV/°C
Gain Error			±0.3		%
Gain Drift vs. Temperature		-5	±2	+5	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN}=50/60Hz, ±2%,	100	110		dB
Common Mode Rejection (CMRR)	f_{IN}=50/60Hz	100	120		dB
Power Supply Rejection(2) (PSRR)	AVDD	75	90		dB
	DVDD	80	120		dB
REFERENCE INPUT					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5		$V_{AVDD} – V_{AVSS}$ + 0.1	V
Absolute Negative Reference Voltage (V_{REFN})		V_{AVSS} – 0.05		V_{REFP} – 0.5	V
Absolute Positive Reference Voltage (V_{REFP})		V_{REFN} + 0.5		V_{AVDD} + 0.05	V
Average Voltage Input Current			75		nA
ADC CLOCK					
External Clock	Frequency Range	1	1.536	1.6	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		1.536		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	$0.8·V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			$0.2·V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7·V_{DVDD}$		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		V_{DGND}		$0.3·V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				±10	μA
POWER SUPPLY					
AVSS Voltage (V_{AVSS})			0		V
AVDD Voltage (V_{AVDD})		2.7		5.25	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD, AVSS Current (I_{AVDD})	Normal Mode		0.6	0.8	mA
	Standby Mode		1		μA
	Power-Down		1		μA

DVDD Current (I_{DVDD})	Normal Mode		170	230	µA
	Standby Mode		20		µA
	Power-Down		1		µA
Total Power Dissipation AVSS Voltage (V_{AVSS})	Normal Mode		3.5		mW
	Standby Mode		0.1		mW
	Power-Down		0.01		mW
TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) Power supply rejection is specified DC change in voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

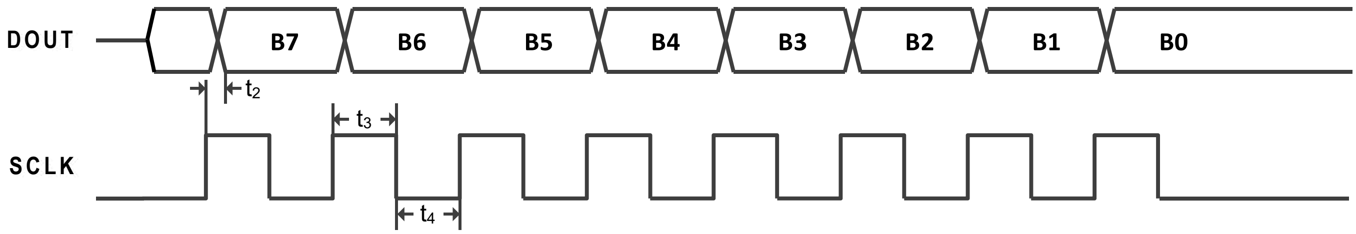


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_2	SCLK rising edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK high pulse width	200		ns
t_4	SCLK low pulse width	200		ns
	SCLK period	400	10^6	ns

(1) DOUT load = 20pF || 100k Ω to DGND.

NOISE PERFORMANCE

Table 1 and Table 2 show ADC noise performance in root mean square (RMS) value, peak-to-peak values, effective number of bits (ENOB), and noise-free bits. The ENOB and noise-free bits listed in the tables are calculated using Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(\mathbf{00.55} \cdot V_{REF}/\text{Gain}/V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(\mathbf{00.55} \cdot V_{REF}/\text{Gain}/V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

Table 1. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V

Data Rate	Gain	RMS Noise(nV)	Peak-to-Peak Noise(nV)	ENOB(RMS)	Noise-Free Bits
10SPS	64	40	222	20.9	18.4
10SPS	128	32	149	20.2	18.0
80SPS	64	100	595	19.6	17.0
80SPS	128	85	483	18.8	16.3

Table 2. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 3 V

Data Rate	Gain	RMS Noise(nV)	Peak-to-Peak Noise(nV)	ENOB(RMS)	Noise-Free Bits
10SPS	64	40	222	20.2	17.7
10SPS	128	32	149	19.5	17.3
80SPS	64	100	595	18.8	16.3
80SPS	128	85	483	18.1	15.6

CIRCUIT DESCRIPTION

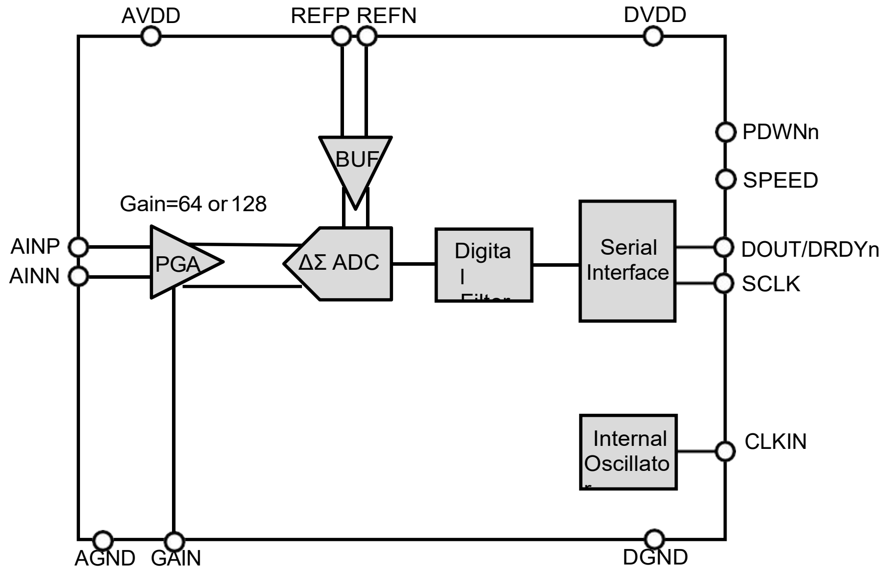


Figure 2. GX1230A Block Diagram

OVERVIEW

The GX1230A is low noise, low drift, and high-resolution 20-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA). The ADC provides high-accuracy measurement solutions for bridge sensors. Figure 2 shows the device block diagram.

The ADC features a high input-impedance, low-noise, programmable gain amplifier (PGA). The PGA gain is selectable with 64 or 128 by GAIN input pin.

A delta-sigma modulator measures the PGA output voltage according to the buffered reference voltage to provide high speed bitstream to the digital filter. Unlike SAR ADCs, this ADC is much easier to drive due to very high impedance at both analog and reference inputs.

The digital filter provides SINC4 filter mode, allowing good line-cycle rejection. Two data rates are provided from the device: 10SPS and 80SPS.

The SP-compatible serial interface is used to read the conversion data. The serial interface consists of two signals: SCLK and DOUT/DRDYn. The DOUT/DRDYn pin serves as dual function of register and ADC data output and also the indicator for data ready after the conversion is done. Parity check is provided for data integrity.

The ADC has two clock options: internal oscillator and external clock. The nominal clock frequency is 1.536MHz.

The ADC operates with a single analog power supply with range from 2.7V to 5.25V. The digital power supply range is 2.7 V to 5.25 V.

Programmable Gain Amplifier (PGA)

The ADC features a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). The PGA input is equipped with an electromagnetic-interference (EMI) filter consisting of two 350-Ω input resistors, and two 8pF filter capacitors, as shown in the Figure 3.

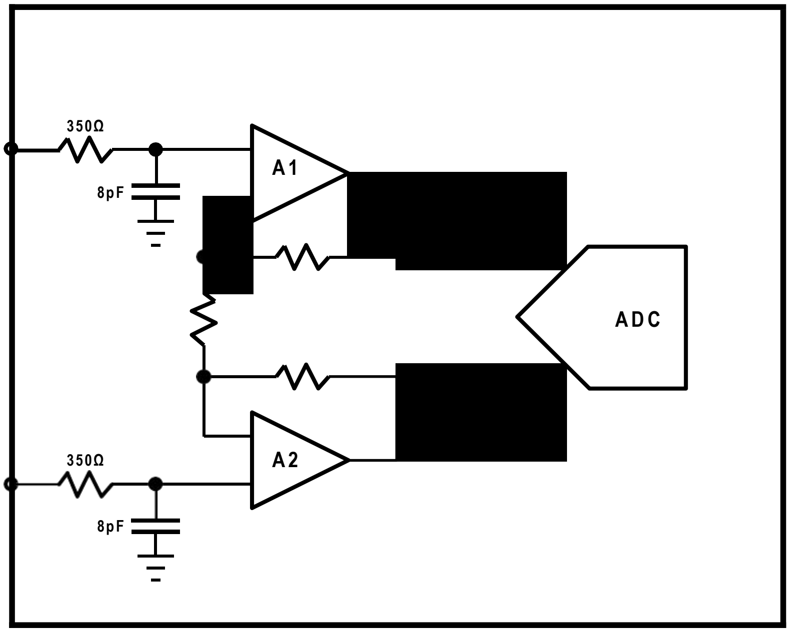


Figure 3. Simplified PGA Block Diagram

The ADC full-scale voltage range is determined by the reference voltage and the PGA gain. Table 3 shows the full-scale voltage range verses gain for 5V reference voltage.

Table 3. ADC Full-Scale Voltage Range with V_{REF} = 5V

GAIN	FULL SCALE RANGE (V)(1)
64	±39 mV
128	±19.5 mV

(1) The full scale input range is proportional to V_{REF}.

Just like most amplifiers, there should be some headroom for the output of PGA to be away from the power supply (V_{AVDD}) and ground (V_{AVSS}) due to the limitation of voltage driving capability of PGA output device as shown in Figure 4. For correct linear operation, the absolute PGA output voltage must locate within the range [V_{AVSS} + 0.5, V_{AVDD} – 0.5]. The analog input common voltage must meet Equation (3):

$$(V_{AVSS} + 0.5 + V_{IN} \cdot Gain) \le V_{CM} \le (V_{AVDD} - 0.5 - V_{IN} \cdot Gain) \quad (3)$$

Where

V_{IN} = differential input voltage = $V_{INP} - V_{INN}$

V_{CM} = input common mode voltage = $(V_{INP} + V_{INN})/2$

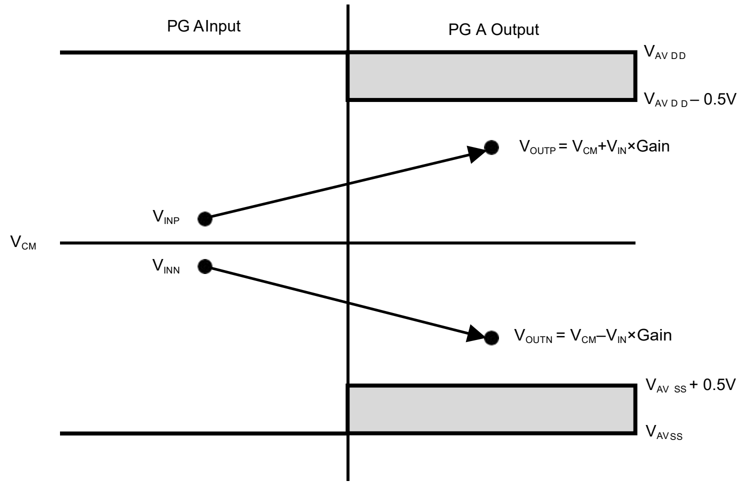


Figure 4. PGA Input and Output Range

Digital Filter and Conversion Time

A delta-sigma (Σ–Δ) ADC consists of a modulator followed by a programmable digital decimation filter to produce the final high-resolution data output. Caution must be taken to choose the type of filtering based on the consideration of tradeoffs between resolution, data rate, line cycle rejection, and conversion latency.

This ADC only provides sinc4 filter. Figure 5 shows the frequency response of the SINC4 and SINC1 filters normalized to output data rate.

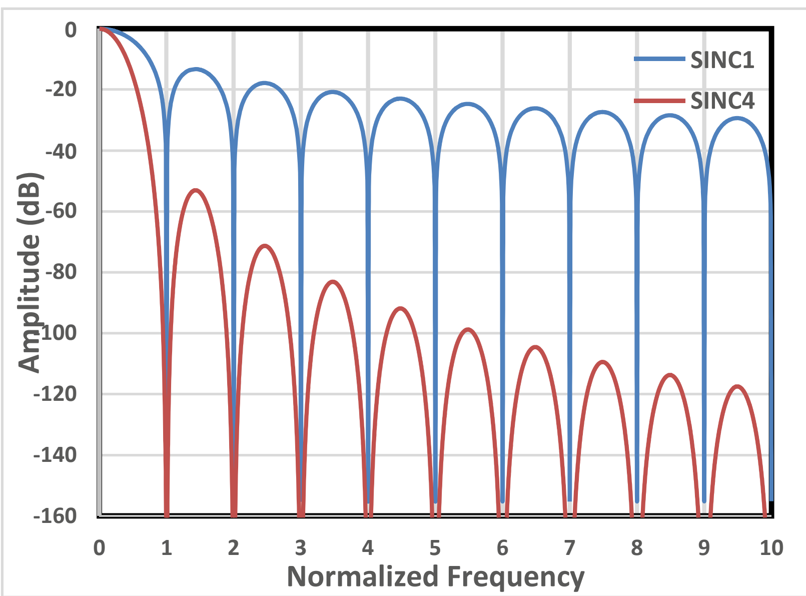


Figure 5. Frequency Response of SINC1/SINC4 Filter

While the order of the SINC filter doesn't affect the notch positions, the higher order SINC4 filter has wider notches resulting in better rejection in the band (±1 Hz) around the notches. The higher order SINC4 filter also gives better stop-band rejection with the tradeoff of longer settling time for the same output data rate. The SINC4 filter normally takes four conversion cycles to settle, while SINC1 filter settles in one conversion cycle.

Clock Mode

The system clock of this ADC can be either from the internal oscillator or provided by external clock source to the CLKIN pin. Figure 6 illustrates the configuration for each clock mode. If the CLKIN pin is shorted to analog ground (AVSS), the internal oscillator is enabled. If an external clock is detected at the CLKIN pin, the ADC automatically selects the external clock.

Option (a) : Internal Oscillator Option (b): External Clock

Figure 6. Clock Mode Configurations

Power-On Reset (POR)

The ADC has two power supplies, analog and digital. The analog power supply (AVDD) range is 2.7V to 5V. The digital supply (DVDD) range is 2.7V to 5V.

Figure 7 shows the POR sequence. The internal POR circuitry forces the ADC in reset state if the digital supply voltage (V_{DVDD}) is below POR voltage threshold which is about 1.3V. After the digital supply voltage (V_{DVDD}) exceeds POR voltage threshold, additional 43 ms of waiting time is needed for power supply to be fully settled before sending any command, otherwise the command is ignored.

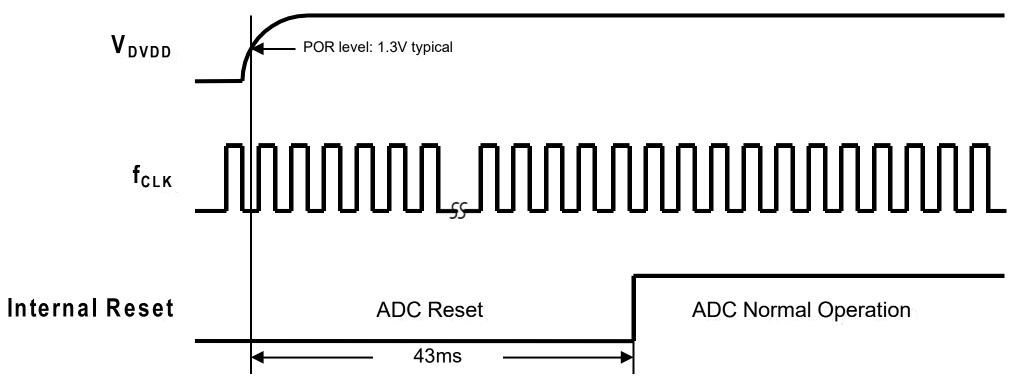


Figure 7. Power-On Reset Sequence

SPI Interface

The ADC provides a 2-wire SPI-compatible interface with SPI Mode 1 supported. Please see Timing Requirements: Serial Interface section for the timing information related to serial interface.

SERIAL CLOCK (SCLK)

The serial clock is a Schmitt-triggered input to make it noise immune. This pin is used to clock data into and out of the device. Output data on DOUT pin are updated on the rising edge of SCLK.

DATA OUTPUT (DOUT/DRDYn)

The DOUT/DRDYn pin is a dual-function output. This pin serves as the serial interface data output and also as an indicator for new data ready for retrieval. First, conversion or register data are shifted out on DOUT/DRDYn pin on the rising edge of SCLK. Second, while the SPI interface is at idle state, the DOUT/DRDYn pin goes low to indicate that new conversion data are ready for retrieval.

Data Format

The device provides 20 bits of conversion data output in binary 2's complement format, left justified, MSB first. The ADC input is bipolar-differential and is scaled such that zero differential input results in an ideal code of 20'h00000, positive full scale input results in an ideal code of 20'h7FFFF, and negative full scale input results in an ideal code of 20'h80000. The output clips if the signal exceeds full-scale. Table 4 lists the ideal output codes for different input signals.

Table 4. Ideal Output Code vs. Input Signal

INPUT SIGNAL VIN = VINP – VINN	IDEAL OUTPUT CODE
≥ FS $(2^{19} – 1) / 2^{19}$	20'h7FFFF
FS / 2^{19}	20'h00001
0	20'h00000
-FS / 2^{19}	20'hFFFFF
≤ –FS	20'h80000

Reading ADC Data

As shown in Figure 8, the ADC data is 3 bytes long with 4-bit of LSB fixed to 4'b1111 after 20-bit conversion data, DATA [19:0]. Parity byte is appended to the conversion data bytes after more than 24 SCLKs is applied. Part of parity byte is formed by the checksum byte, which is the 8-bit sum of data conversion bytes plus an offset value, 8'h5B. The first and last bit of parity byte are forced with 1'b1.

CHECKSUM [7:0] = DATA [19:12] + DATA [11:4] + {DATA [3:0], 4'b1111} + 8'h5B

PARITY [7:0] = {1'b1, CHECKSUM [6:1], 1'b1}

After four bytes are read, the data byte sequence is repeated when more SCLKs are sent. The repeating byte sequence starts with the first byte DATA [19:12].

The read operation needs to complete 2 system clock cycles before the next new data is ready, otherwise the retrieved data is corrupted by the updating of new data on DOUT/DRDYn pin.

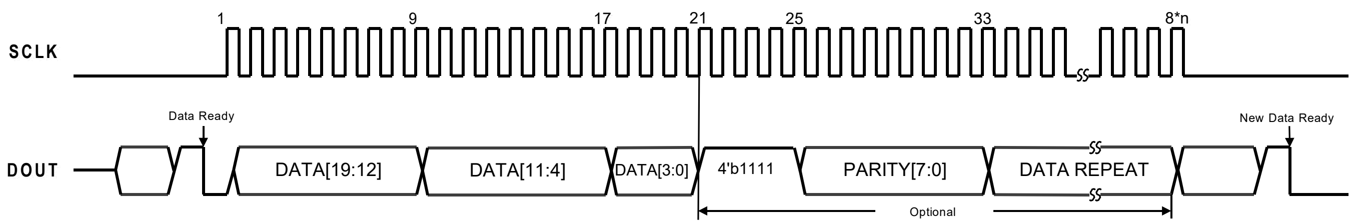


Figure 8. Reading Data Sequence

Standby Mode

In normal conversion mode, it is required to have SCLK low after data retrieval before the next new data is updating with DOUT/DRDYn pin going to high. If user holds SCLK high while the next new data is updating with DOUT/DRDYn pin going to high, the device will enter standby mode to save power with about only 20uA current used. To exit standby mode, set SCLK low. The first data after exiting standby mode is fully settled data after 4x time of data interval.

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May. 20, 2022		Initial release.

DISCLAIMER

GXSC reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

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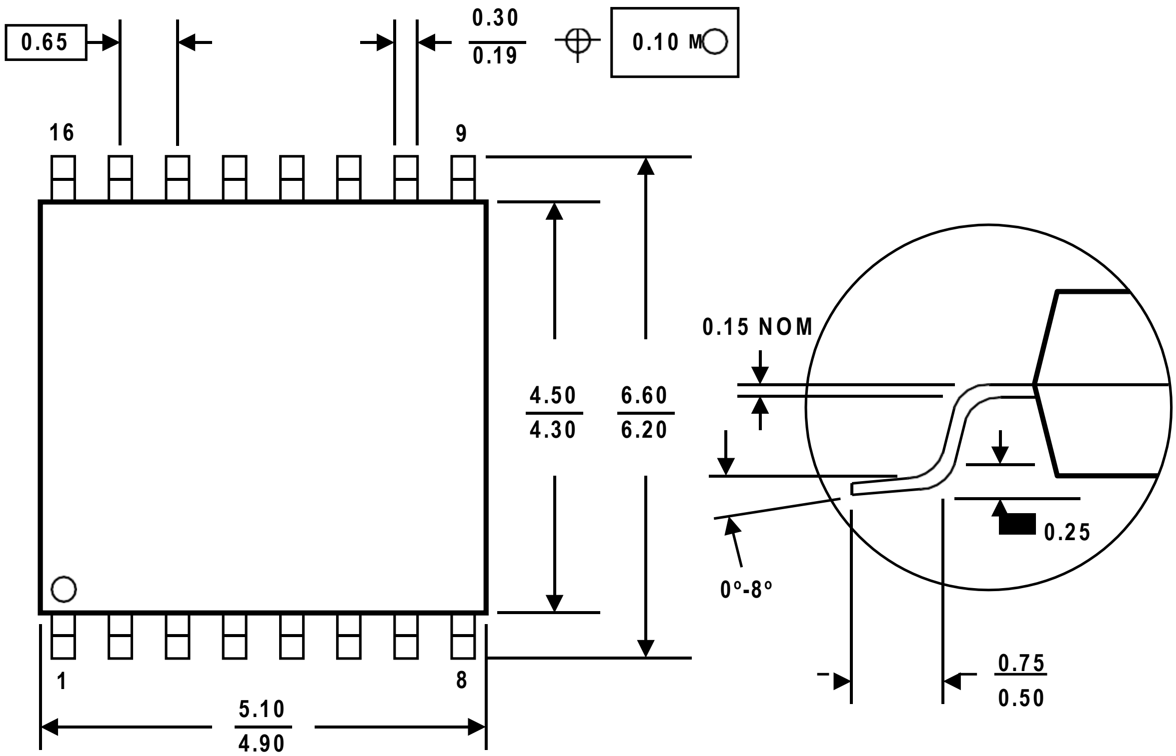
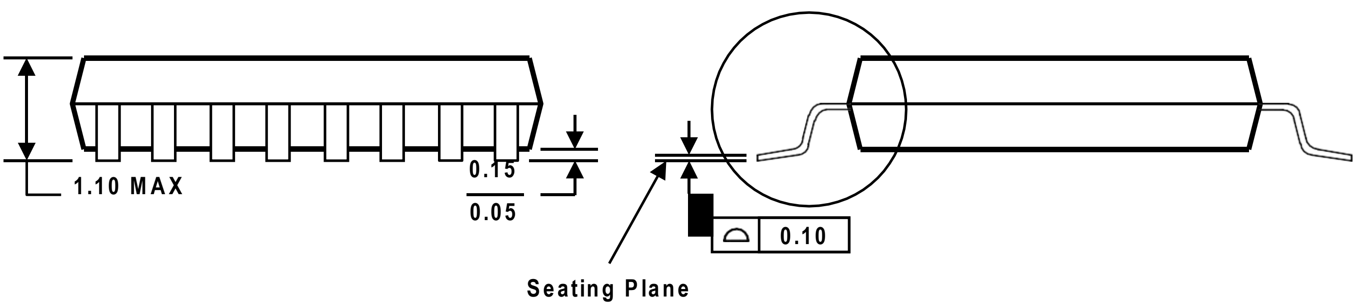
PACKAGE OUTLINE DIMENSIONS





A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to changewithout notice.