GX9251 Dual 14-Bit, 20/40/65/80MSPS ADC

FEATURES

- 1.8 V analog supply operation
- 1.8 V to 3.3 V output supply
- Low power:

32 mW per channel at 20 MSPS

68 mW per channel at 80 MSPS

- SNR:

74.4 dBFS at 30.5 MHz input

70 dBFS at 200 MHz input

- SFDR:

82 dBc at 30.5 MHz input

74 dBc at 200 MHz input

- DNL = ±0.75 LSB (typ)
- On-chip voltage reference and sample-and-hold circuit
- QFN-64 package 9mm×9mm

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
- I/Q demodulation systems
- Smart antenna systems
- Battery-powered instruments
- Hand held scope meters
- Portable medical imaging
- Ultrasound
- Radar/LIDAR

FUNCTIONAL BLOCK DIAGRAM

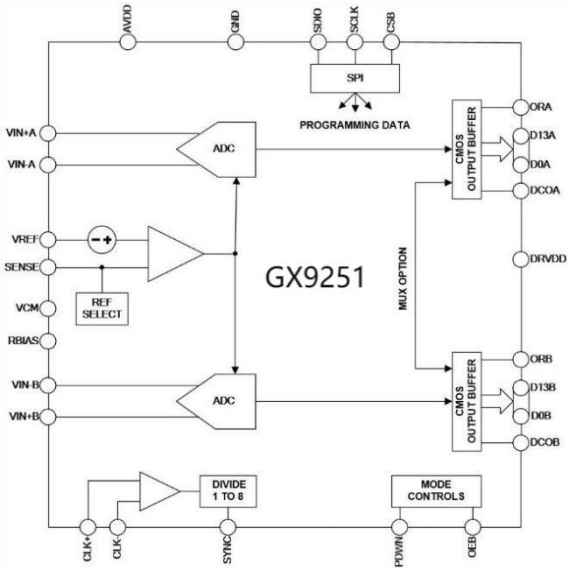

Figure 1. Functional Block Diagram

Version: V1.3
Release Date: 2023/12/05

DESCRIPTION

The GX9251 is a monolithic, dual-channel, 14-bit, 20 MSPS/40 MSPS/65 MSPS/80 MSPS ADC, and operates from a single 1.8V analog power supply. It features a high-performance sample-and-hold circuit and on-chip voltage reference.

The product adopts multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 80 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The GX9251 contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input controls all internal conversion cycles. The digital output data is presented in offset binary, gray code, or twos complement format. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic signal. Both 1.8 V and 3.3 V CMOS levels are supported and output data can be multiplexed onto a single output bus.

The GX9251 is available in a 64-lead RoHS compliant QFN.

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SPECIFICATIONS

ADC DC Characteristics

AVDD = 1.8 V, DRVDD = 1.8 V, 80MSPS sampling rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 1. ADC DC characteristics

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Resolution			14		Bits
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±0.1	±0.7	%FSR
Gain Error	Full		-1.5		%FSR
Differential Nonlinearity (DNL)[1]	Full 25°C	-0.75	 ±0.45	0.75	LSB LSB
Integral Nonlinearity (INL)[1]	Full 25°C	-2.5	 ±1.0	2.5	LSB LSB
Internal Voltage Reference Error	Full		±5		mV
Input-referred Noise (V_{REF}=1V)	25°C		0.98		LSB rms
Analog Input Range (V_{REF}=1V)	Full		2		V_{PP}
Input Capacitance[2]	Full		4		pF
Input Common-Mode Voltage	Full		0.95		V
AVDD Power Supply	Full	1.7	1.8	1.9	V
DRVDD Power Supply	Full	1.7		3.6	V
I_{AVDD} Power Supply Current	Full		78	86	mA
I_{DRVDD1} Power Supply Current (1.8V) I_{DRVDD2} Power Supply Current (3.3V)	Full		7 15		mA mA
DC Input Power Consumption	25°C		136		mW
Sine Wave Input Consumption [1] (DRDVV=1.8V) Sine Wave Input Consumption [1] (DRDVV=3.3V)	Full		153 194		mW mW
Power-Down Power	25°C		2		mW

1. Measured with a 10MHz input frequency at rated sample rate, full scale sine wave, with approximately 5pF loading on each output bit.
2. Input capacitance refers to the effective capacitance between a differential input pin and AGND.

ADC AC Characteristics

AVDD = 1.8 V, DRVDD = 1.8 V, 80MSPS sampling rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 2. ADC AC characteristics

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Signal-to-Noise Ratio (SNR)					
f_{in}=30.5MHz	25°C		74.4		dBFS
f_{in}=70MHz	25°C		72.7		dBFS
	Full	72.2			dBFS
f_{in}=140MHz	25°C		71		dBFS
f_{in}=200MHz	25°C		70.1		dBFS
Signal-to-Noise Distortion Ratio (SNDR)					
f_{in}=30.5MHz	25°C		74.3		dBFS
f_{in}=70MHz	25°C		72.5		dBFS
	Full	72		73.3	dBFS
f_{in}=140MHz	25°C		70.6		dBFS
f_{in}=200MHz	25°C		70		dBFS
Effective Number of Bits (ENOB)					
f_{in}=30.5MHz	25°C		12		Bits
f_{in}=70MHz	25°C		11.8		Bits
	Full	11.7			Bits
f_{in}=140MHz	25°C		11.5		Bits
f_{in}=200MHz	25°C		11.3		Bits
Spurious-free Dynamic Range (Third Harmonic)					
f_{in}=30.5MHz	25°C		86.6		dBc
f_{in}=70MHz	25°C		85		dBc
	Full	81.6			dBc
f_{in}=140MHz	25°C		83		dBc
f_{in}=200MHz	25°C		73.4		dBc
Spurious-free Dynamic Range (Second Harmonic)					
f_{in}=30.5MHz	25°C		82		dBc
f_{in}=70MHz	25°C		88.6		dBc
	Full	85.6			dBc
f_{in}=140MHz	25°C		78		dBc
f_{in}=200MHz	25°C		73		dBc
Crosstalk[1]	Full		-100		dB
Analog Input Bandwidth	25°C		700		MHz

1.Crosstalk is measured at 70 MHz with −1.0 dBFS on one channel and no input on the adjacent channel.

Digital Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, 80MSPS sampling rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 3. Digital Specifications Parameter

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Differential Clock Inputs (CLK+/-)					
Logic Compliance	Full		CMOS/LVDS/LVPECL		
Internal Common Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V
Input Voltage Range	Full	GND-0.3		AVDD+0.2	V
Input Resistance	Full		8		kΩ
Input Capacitance	Full		3.5		pF
LOGIC INPUTS (PDWN,SYNC,SCLK,CSB,SDIO)					
Logic 1 Voltage	Full	1.2		DRVDD+0.3	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
DIGITAL OUTPUTS DRVDD = 1.8V					
Logic 1 Voltage	Full	1.79			V
Logic 0 Voltage	Full			0.2	V
DRVDD = 3.3V					
Logic 1 Voltage	Full	3.29			V
Logic 0 Voltage	Full			0.2	V
Encoding Format (Default)			Offset binary		

Timing Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, 80MSPS sampling rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 4. Switching Parameter

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Clock Input Parameter					
Input Clock Rate	Full			625	MHz
Conversion Rate	Full			80	MHz
Aperture Delay (t_A)	Full		1		ns
Aperture Uncertainty	Full		0.1		ps rms
Data Output Parameters					
t_A	Full		1		ns
t_{CH}	Full		6.25		ns
t_{CLK}	Full		12.5		ns
t_{DCO}	Full		3		ns
t_{PD}	Full		3		ns
t_{SKEW}	Full		0.1		ns

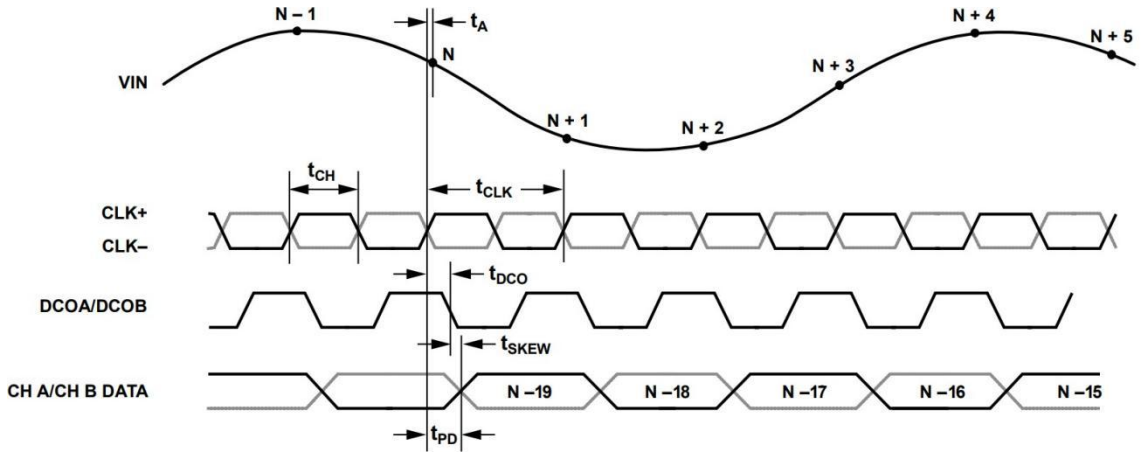


Figure 2. CMOS Output Data Timing

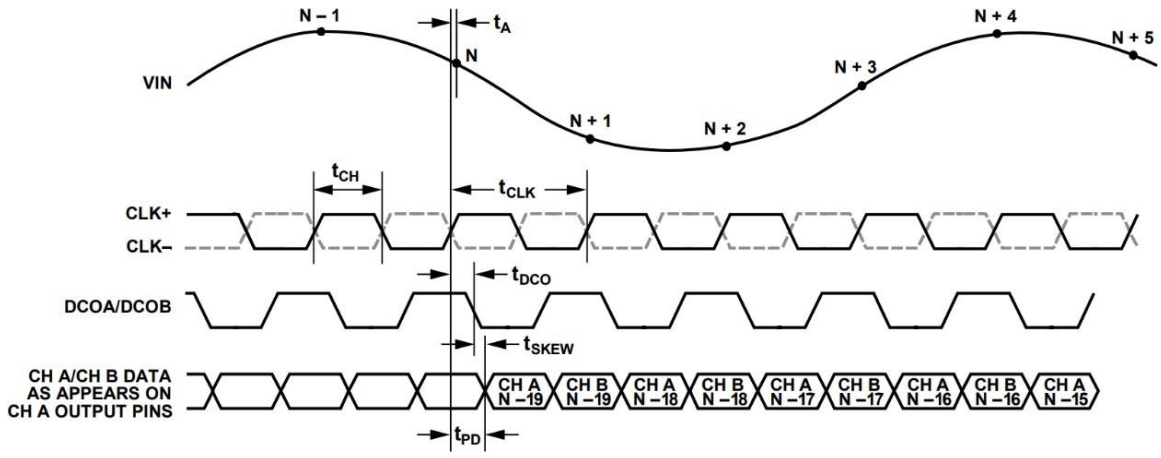


Figure 3. CMOS Interleaved Output Timing, Output as Appears on Channel A Output Pins

Table 5. SPI Timing Parameter

PARAMETER	CONDITION	LIMIT
t_{DS}	Setup time between the data and the rising edge of SCLK	2ns, min
t_{DH}	Hold time between the data and the rising edge of SCLK	2ns, min
t_{CLK}	Period of the SCLK	40ns, min
t_S	Setup time between CSB and SCLK	2ns, min
t_H	Hold time between CSB and SCLK	2ns, min
t_{HIGH}	SCLK pulse width high	10ns, min
t_{LOW}	SCLK pulse width low	10ns, min

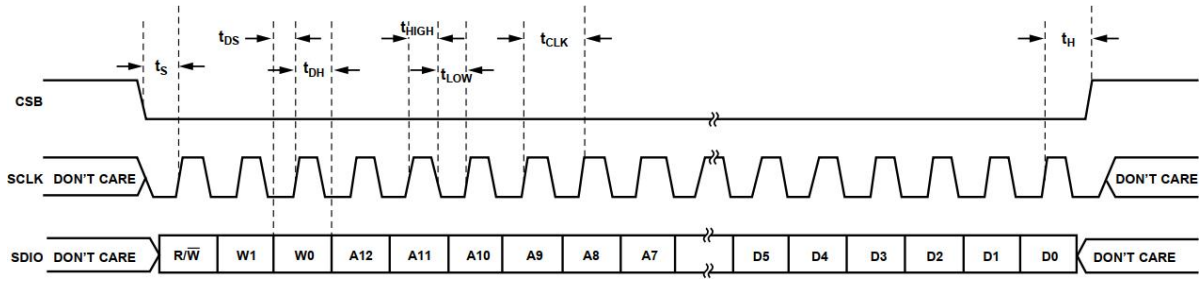


Figure 4. Serial Port Interface Timing

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND……-0.3V to 2V

DRVDD to AGND……-0.3V to 3.9V

Input Voltage (VIN+/-,CLK+/-,VREF,SENSE,VCM,RBIAS)……-0.3V to AVDD+0.2V

Input Voltage (CSB, SCLK, SDIO, PDWN)……-0.3V to DRVDD+0.3V

Output Voltage (DCOA,DCOB,D0A/D0B to D13A/D13B)……-0.3V to DRVDD+0.3V

Maximum Junction Temperature $T_{J,MAX}$……150°C

Operating Temperature Range……-40°C to 85°C

Storage Temperature Range……-65°C to 150°C

ESD (Human Body Model) ……2000V

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

ESD CAUTION

This product is an electrostatic sensitive device. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

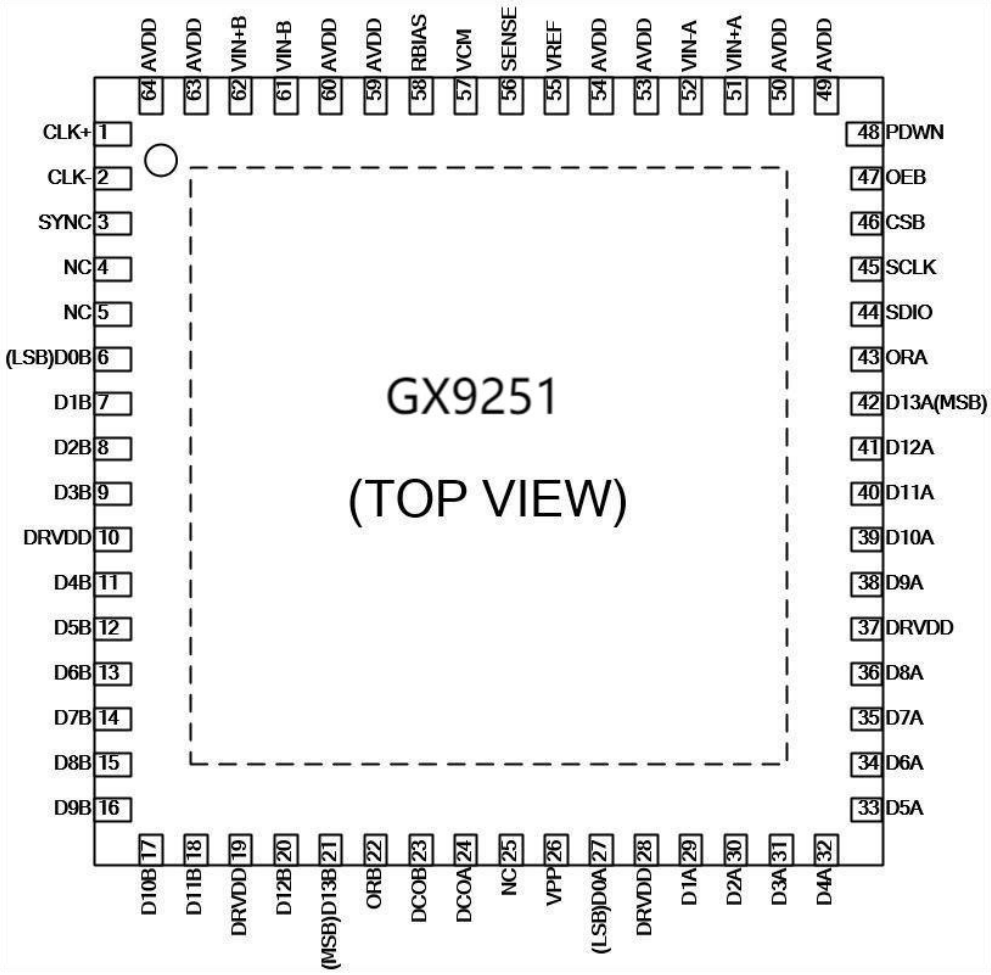


Figure 5. Pin (pad) Configuration

Table 6. Pin Definition

Pin No.	Pin Name	Pin Function
0	GND	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation
1,2	CLK−, CLK+	Differential Encode Clock
3	SYNC	Digital Input. SYNC input to clock divider
4,5,25,26	NC	Do Not Connect.
6 to 9, 11 to 18, 20, 21	D0B to D13B	Channel B Digital Outputs
10, 19, 28, 37	DRVDD	Digital Output Driver Supply, 1.8V to 3.3V
22	ORB	Channel B Out-of-Range Digital Output
23	DCOB	Channel B Data Clock Digital Output
24	DCOA	Channel A Data Clock Digital Output
27, 29 to 36, 38 to 42	D0A to D13A	Channel A Digital Outputs

Pin No.	Pin Name	Pin Function
43	ORA	Channel A Out-of-Range Digital Output
44	SDIO	SPI Data Input/Output
45	SCLK	SPI Clock Input
46	CSB	SPI Chip Select. Active low enable; 30 kΩ internal pull-up
47	OEB	Digital Input. Enable Channel A and Channel B digital outputs if low, tristate outputs if high. 30 kΩ internal pull-down
48	PDWN	Digital Input. 30 kΩ internal pull-down PDWN high = power-down device PDWN low = run device, normal operation
49, 50, 53, 54, 59, 60, 63, 64	AVDD	1.8 V Analog Supply
51,52	VIN+A,VIN−A	Channel A Analog Inputs
55	VREF	Voltage Reference Input/Output
56	SENSE	Reference Mode Selection
57	VCM	Analog common mode input
58	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground
61,62	VIN−B,VIN+B	Channel B Analog Input

TYPICAL CURVE

AVDD = 1.8 V, DRVDD = 1.8 V, TA=27ºC, VIN = -1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

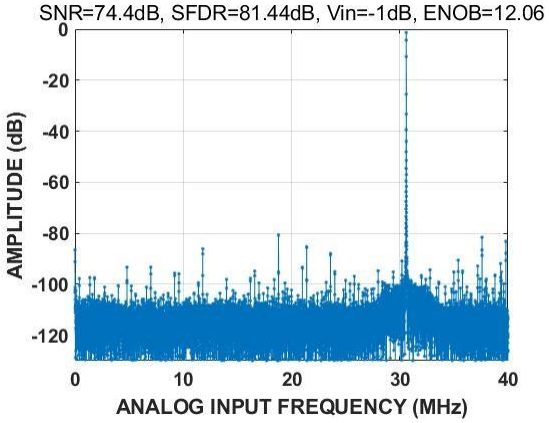


Figure 6. Single-Tone FFT (fin = 30.5MHz@80MSPS)

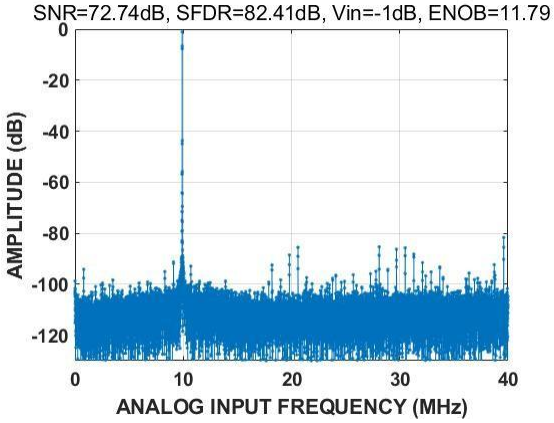


Figure 7. Single-Tone FFT (fin = 70MHz@80MSPS)

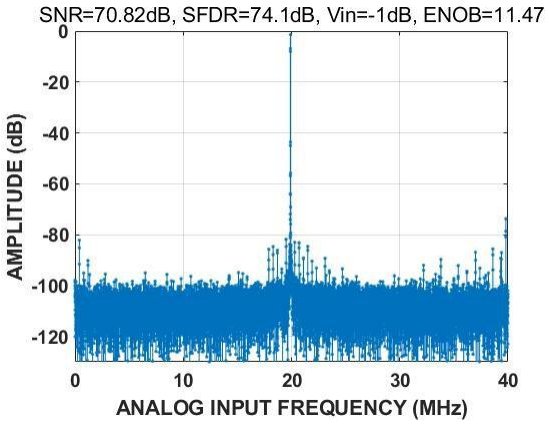


Figure 8. Single-Tone FFT (fin = 140MHz@80MSPS)

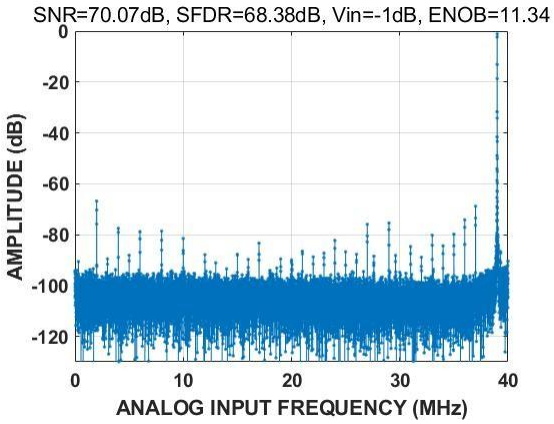


Figure 9. Single-Tone FFT (fin = 200MHz@80MSPS)

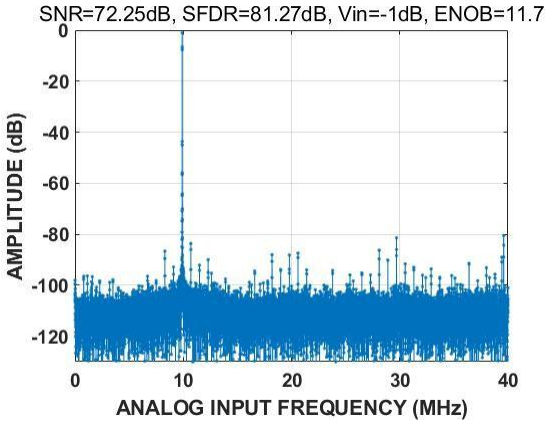


Figure 10. Single-Tone FFT (fin = 70MHz@80MSPS) High Temperature (+125℃)

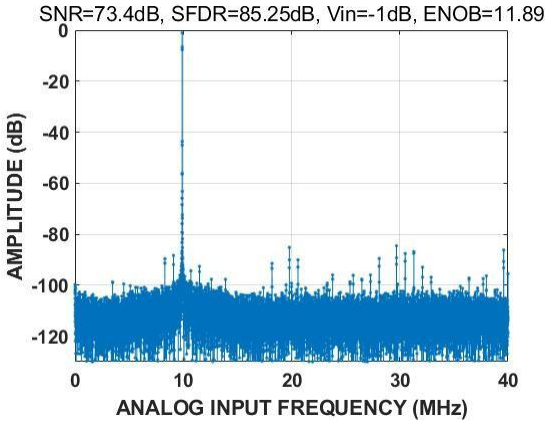


Figure 11. Single-Tone FFT (fin = 70MHz@80MSPS) Low Temperature (-40℃)

TYPICAL APPLICATION CIRCUIT

The typical application circuits of peripheral devices such as GX9251 input signal, input clock, and external DC pins are as follows.

Analog Input Network

The optimal performance of ADC is achieved through differential driving of analog inputs. For baseband applications below ~10 MHz where SNR is a key parameter, differential transformer-coupling is the recommended input configuration (see Figure 13). To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer. At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the GX9251.

For applications above ~10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 12).

Using the input network method of VIN- connected to common mode voltage and VIN+ connected to input signal can cause the chip SNR to deteriorate, so it is not recommended to drive GX9251 input with a single end.

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 7 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

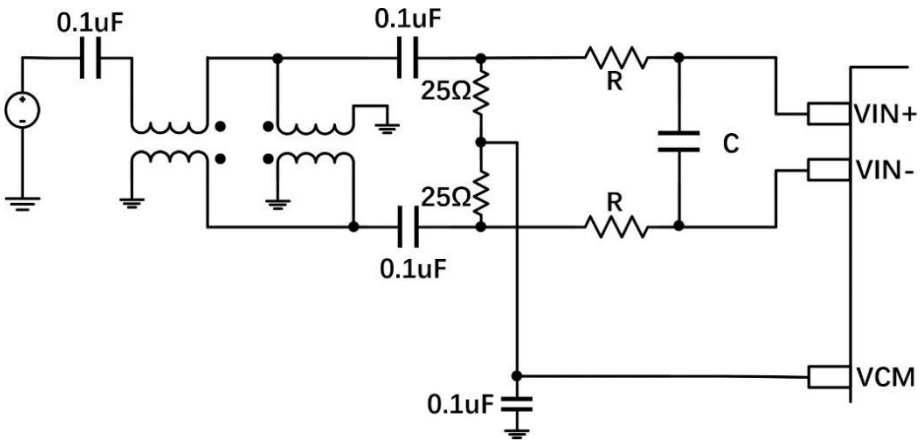


Figure 12. Differential Double Balun Input Configuration

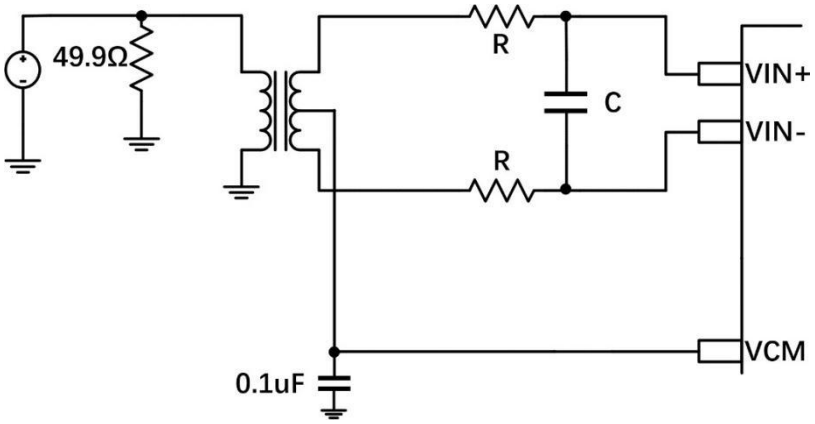


Figure 13. Differential Transformer-Coupled Input Configuration

Table 7. Example RC Network

Frequency Range (MHz)	R (Ω)	C Differential (pF)
0 to 70	33	22
70 to 200	125	Open

Clock Input Network

To fully utilize the performance of the chip, a differential signal should be used as the clock signal of the GX9251 sampling clock input (CLK+/-). The input clock pin has internal bias and does not require external bias. Suggest sampling the configuration of the RF transformer, as shown in Figure 14. The back-to-back Schottky diode connected to the transformer can limit the clock signal input to GX9251 to approximately 0.8V differential peak to peak. In this way, not only can the large voltage swing of the clock be prevented from feeding to other parts, but also the fast rise and Fall time of the signal can be reserved, which is very important for low jitter performance.

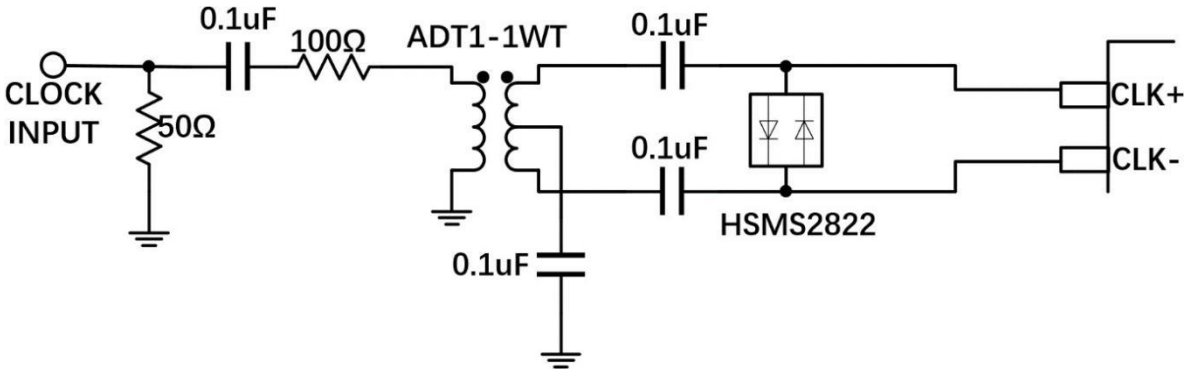


Figure 14. Clock Input Configuration

Reference Configuration Method

A comparator within the GX9251 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 8. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider, setting VREF to 1.0 V. If the internal reference of the GX9251 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference must be limited to a maximum

of 1.0 V. It is not recommended to leave the SENSE pin floating.

Table 7. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting V_{REF} (V)	Resulting Differential Span (V_{PP})
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0

Digital Outputs Format

The GX9251 output drivers can be configured to interface with 1.8 V to 3.3 V CMOS logic families. Output data can also be multiplexed onto a single output bus to reduce the total number of traces required; the timing is shown in Figure 2. The output driver should be able to provide sufficient output current to drive various logic circuits, and the driving force can be adjusted through registers. However, high driving current may cause spurious pulses in the power signal, affecting the performance of the converter. Therefore, in applications that require ADC to drive large capacity loads or large fanouts, external buffers or latches may be required.

Table 9. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode	OR
VIN+ - VIN-	< -VREF – 0.5LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ - VIN-	= -VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ - VIN-	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ - VIN-	= +VREF – 1LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ - VIN-	> +VREF – 0.5LSB	11 1111 1111 1111	01 1111 1111 1111	1

Digital Output Enable Function (OEB)

The GX9251 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the OEB pin or through the SPI interface. If the OEB pin is low, the output data drivers and DCOs

are enabled. If the OEB pin is high, the output data drivers and DCOs are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage. When using the SPI interface, the data outputs and DCO of each channel can be independently three-stated by using the output disable (OEB) bit (Bit 4) in Register 0x14.

Timing

The GX9251 provides latched data with a pipeline delay of 9 clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Minimize the length of the output data lines and loads placed on them to reduce transients within the GX9251. These transients can degrade converter dynamic performance. The lowest typical conversion rate of the GX9251 is 3 MSPS. At clock rates below 3 MSPS, dynamic performance can degrade.

Data Clock Output (DCO)

The GX9251 provides two data clock output (DCO) signals intended for capturing the data in an external register. The CMOS data outputs are valid on the rising edge of the DCO, unless the DCO clock polarity has been changed via the SPI. See Figure 2 and Figure 3 for a graphical timing description.

Built-in Self-test (BIST)

The BIST is a thorough test of the digital portion of the selected GX9251 signal path. Perform the BIST test after a reset to ensure the part is in a known state. During BIST, data from an internal pseudorandom noise (PN) source is driven through the digital datapath of both channels, starting at the ADC block output. At the datapath output, CRC logic calculates a signature from the data. The BIST sequence runs for 512 cycles and then stops.

Once completed, the BIST compares the signature results with a pre- determined value. If the signatures match, the BIST sets Bit 0 of Register 0x24, signifying the test passed. If the BIST test fails, Bit 0 of Register 0x24 is cleared. The outputs are connected during this test, so the PN sequence can be observed as it runs. Writing the value 0x05 to Register 0x0E runs the BIST. This enables the Bit 0 (BIST enable) of Register 0x0E and resets the PN sequence generator, Bit 2 (BIST INIT) of Register 0x0E. At the completion of the BIST, Bit 0 of Register 0x24 is automatically cleared.

The PN sequence can be continued from its last value by writing a 0 in Bit 2 of Register 0x0E. However, if the PN sequence is not reset, the signature calculation does not equal the predetermined value at the end of the test. At that point, the user needs to rely on verifying the output data.

Output Test Modes

The output test options are described in Table 10 at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block.

Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock.

SERIAL PORT INTERFACE (SPI)

The GX9251 Serial Port Interface (SPI) allows users to configure the corresponding function registers inside the ADC to meet specific functional and operational needs. Through the serial port, the address space can be accessed and read and written. Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin. The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles. The timing requirements are shown in Figure 4.

Memory Map Register Table

Table 10. Memory Map Register Table

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
0x00	port configuration	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	LSB or MSB mode register
0x01	Chip ID	chip ID 0x23								0x23	Unique chip ID used to differentiate devices; read only.
0x02	Chip grade		000 = 20 MSPS 001 = 40 MSPS 010 = 65 MSPS 011=80MSPS								Unique speed grade ID used to differentiate devices; read only
0x05	Channel index							Data Channel B	Data Channel A	0x03	Determines which device on chip

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
											receives the next write command. The default is all devices on chip
0x08	Mode	External Power-down enable	External pin function 0x00full power-down 0x01 standby					00 = chip run 01 = full power-down 10 = standby 11 = digital reset		0x80	Determines various generic modes of chip operation.
0x0B	Clock divide						Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 1 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 5 110 = divide by 6 111 = divide by 7			0x00	
0x0D	Test mode	User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once		Reset PN long sequence	Reset PN short sequence	Output test mode:0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle 1000 = user input				0x00	When set, the test data is placed on the output pins in place of normal data.

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
						1001 = 1-/0-bit toggle 1010 = 1x sync 1011 = one bit high 1100 = mixed bit frequency					
0x0E	BIST enable						BIST INIT		BIST enable	0x00	Whether to activate BIST function
0x10	Offset adjust	8-bit device offset adjustment [7:0] Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Device offset trim
0x14	ADC Output mode	00 = 3.3 V CMOS 10 = 1.8 V CMOS			Output disable		Output Invert	00 = offset binary 01 = twos complement 10 = gray code 11 = offset binary		0x00	Configures the outputs and the format of the data
0x15	OUTPUT_ADJUST	3.3 V DCO drive strength 00 = 1 stripe (default) 01 = 2 stripes 10 = 3 stripes 11 = 4 stripes		1.8 VDCO drive strength 00 = 1 stripe 01 = 2 stripes 10 = 3 stripes (default) 11 = 4 stripes		3.3 V data drive strength 00 = 1 stripe (default) 01 = 2 stripes 10 = 3 stripes 11 = 4 stripes		1.8 V data drive strength 00 = 1 stripe 01 = 2 stripes 10 = 3 stripes(default) 11 = 4 stripes		0x22	Determines CMOS output drive strength properties
0x16	OUTPUT_PHASE	DCO output polarity 0 = normal 1 = inverted					Input clock phase adjust [2:0] (Value is number of input clock cycles of phase delay) 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles			0x00	On devices that utilize global clock divide, determines which phase of the divider

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
							101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles				output is used to supply the output clock; internal latching is unaffected
0x17	OUTPUT_DELAY		DATA_Delay 000 = 0.56 ns 001 = 1.12 ns 010 = 1.68 ns 011 = 2.24 ns 100 = 2.80 ns 101 = 3.36 ns 110 = 3.92 ns 111 = 4.48 ns				DCO_Delay 000 = 0.56 ns 001 = 1.12 ns 010 = 1.68 ns 011 = 2.24 ns 100 = 2.80 ns 101 = 3.36 ns 110 = 3.92 ns 111 = 4.48 ns			0x00	This sets the fine output delay of the output clock but does not change internal timing
0x19	USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 1 LSB
0x1A	USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 1 MSB
0x1B	USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 2 LSB
0x1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 2 MSB

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
0x24	MISR_LSB								B0	0x00	Least significant byte of MISR; read only
0x2A	Features								OR Output Enable	0x01	Disable the OR pin for the indexed channel
0x2E	Output assign								0 = ADC A 1 = ADC B	Ch A = 0x00 Ch B = 0x01	Assign an ADC to an output channel
0x3C	Interleave mode control						Interleaved output enable			0x00	Interleave mode control
0x100	Sync control						Clock divider next sync only	Clock divider sync enable	Master sync enable	0x01	
0x101	USR2	Enable OEB Pin 47								0x80	

APPLICATION INFORMATION

Power and Ground Recommendations

it is recommended that two separate power supplies are used for the GX9251. one is for analog power (AVDD),the other is for digital power (DRVDD). For AVDD and DRVDD, several different decoupling capacitors should be used to reduce high and low frequencies noise. these capacitors should be close to the pins of the device with minimal trace length. A single PCB ground plane is sufficient for the GX9251. With proper decoupling and being isolated between sections of analog, digital, and clock, optimum performance is easily achieved.

Exposed Pad Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. continuous exposed (no solder mask) copper plane on the PCB should match the GX9251 exposed paddle.

The copper plane should have as much as through vias to achieve as lower as thermal resistance for heat dissipation. These vias should be filled to prevent solder wicking. To optimized adhere the ADC to the PCB, silkscreen is recommended to partition the continuous plane on the PCB into several uniform sections that provide several tie points between the ADC and the PCB during the reflow process. Since there is only one connection point between the ADC and the PCB Using one continuous plane with no partitions.

VCM

The VCM pin must be decoupled to ground with a 0.1 μF capacitor.

RBIAS

The GX9251 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

Reference Decoupling

The VREF pin must be externally decoupled to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

SPI Port

The SPI port must not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the SPI bus is used for other devices on-PCBA, it may be necessary to provide buffers between this bus and the GX9251 to keep these signals from transitioning at the converter inputs during critical sampling periods.

Data Output

Due to circuit structure issues, if there is a requirement for a fixed data output delay, there is a power on timing requirement (it is necessary to power on the DRVDD's power then wait a few milliseconds before powering on the AVDD). If data synchronization output between channels is required, the data output path needs to be reset as follows:

SPI_Write (0x08 0x03);

SPI_Write (0x08 0x00);

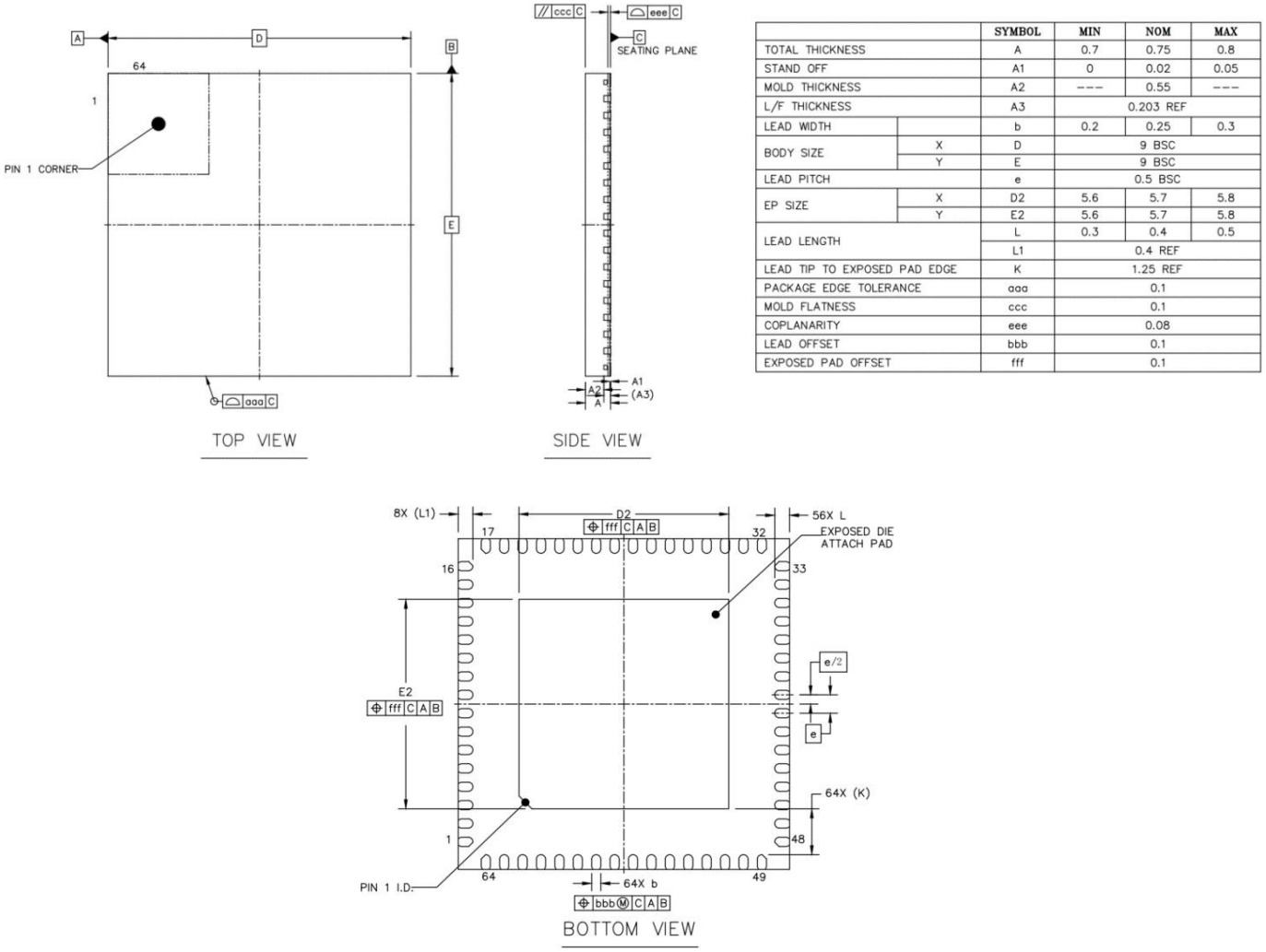
ORDERING GUIDE

Table 11. Order Information

Part No.	Temperature Range	Package
GX9251GDLUMZ-20	-40 ~ 85℃	QFN-64
GX9251GDLUMZ-40	-40 ~ 85℃	QFN-64
GX9251GDLUMZ-65	-40 ~ 85℃	QFN-64
GX9251GDLUMZ-80	-40 ~ 85℃	QFN-64

Customed packages are available.

OUTLINE DIMENSION



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5.6	5.7	5.8
	Y	E2	5.6	5.7	5.8
LEAD LENGTH		L	0.3	0.4	0.5
		L1		0.4 REF	
LEAD TIP TO EXPOSED PAD EDGE		K		1.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Figure 15. 64 Pin QFN (Dimension shown in millimeter)

DECLARATION

The information above is for reference only and is intended to assist GXSC (Shenzhen) Technology Co., Ltd customers in their design and development. GXSC (Shenzhen) Technology Co., Ltd reserves the right to change the above information without prior notice due to technological innovation.

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