GX9253 Quad, 14-Bit, 80/105/125MSPS ADC

FEATURES

- 1.8 V supply operation
- Low power: 110 mW per channel at 125MSPS
- SNR: 73 dB (to Nyquist)
- DNL: ±0.75 LSB (typical)
- INL: ±2.5 LSB (typical)
- Serial LVDS
- $2V_{P-P}$ input voltage range
- QFN-48 package 7mm×7mm

APPLICATIONS

- Medical Ultrasound
- Test equipment
- Radio receivers
- Fiber network

FUNCTIONAL BLOCK DIAGRAM

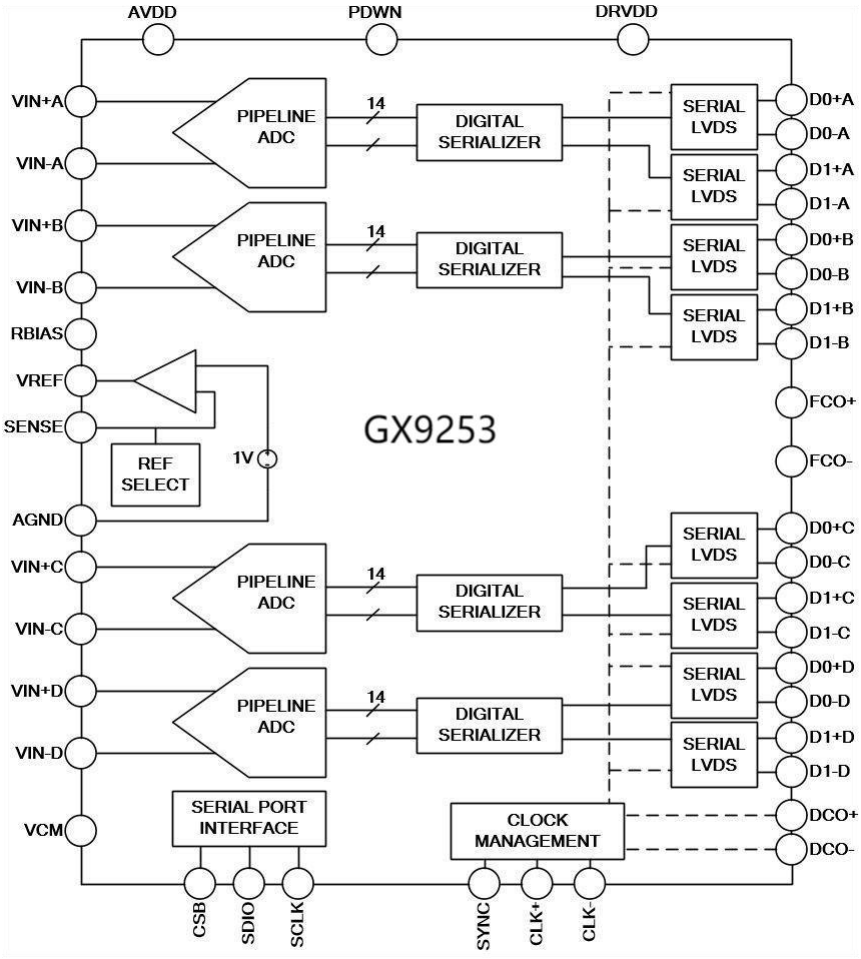

Figure 1. Functional Block Diagram

Version: V1.4
Released Date: 2024/03/07

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DESCRIPTION

The GX9253 is a quad, 14-bit, 80 MSPS/105 MSPS/125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and has outstanding dynamic performance and low power consumption characteristics.

The ADC requires a single 1.8 V power supply and LVPECL-/ CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes 2.2 mW when all channels are disabled.

The GX9253 is available in a RoHS-compliant, 48-lead QFN.

SPECIFICATIONS

ADC DC CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, 125MSPS sampling rate, VIN = -1.0 dBFS, 1.0 V internal reference, unless otherwise noted.

Table 1. ADC DC characteristics

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Resolution			14		Bits
No Missing Codes	Full		Guaranteed		
Offset Error	Full	-0.7	-0.3	+0.1	%FSR
Gain Error	Full	-10	-5	0	%FSR
Differential Nonlinearity (DNL)[1]	Full 25℃	-2.0	 ±0.75	+2.0	LSB LSB
Integral Nonlinearity (INL)[1]	Full 25℃	-5.0	 ±2	+5.0	LSB LSB
Internal Voltage Reference Error	Full		±5		mV
Input-referred Noise (V_{REF}=1V)	25℃		0.94		LSB rms
Analog Input Range (V_{REF}=1V)	Full		2		V_{PP}
Input Capacitance[2]	Full		3		pF
Input Common-Mode Voltage	Full		0.95		V
AVDD Power Supply	Full	1.7	1.8	1.9	V
DRVDD Power Supply	Full	1.7	1.8	1.9	V
I_{AVDD} Power Supply Current	Full		273.1		mA
I_{DRVDD} Power Supply Current (ANSI-644 Mode)	Full		70.2		mA
DC Input Power Consumption	25℃		591.5		mW
Sine Wave Input Consumption [1] (ANSI-644 Mode)	Full		617.9		mW
Sine Wave Input Consumption [1] (Reduced Rang Mode)	Full		573.7		mW
Power-Down Consumption	25℃		2.2		mW

1. The measurement conditions: 10MHz input frequency, full scale sine wave, and a load of approximately 5pF for each output.
2. Input capacitance refers to the effective capacitance between a differential input pin and AGND.

ADC AC CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, 125MSPS sampling rate, VIN = -1.0 dBFS, 1.0 V internal reference, unless otherwise noted.

Table 2. ADC AC characteristics

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Signal-to-Noise Ratio (SNR)					
f_{in}=30.5MHz	25°C		73		dBFS
f_{in}=70MHz	25°C		71.1		dBFS
	Full	70.3			dBFS
f_{in}=140MHz	25°C		68.6		dBFS
f_{in}=200MHz	25°C		68.5		dBFS
Signal-to-Noise Distortion Ratio (SNDR)					
f_{in}=30.5MHz	25°C		72.7		dBFS
f_{in}=70MHz	25°C		71		dBFS
	Full	70.2			dBFS
f_{in}=140MHz	25°C		68.5		dBFS
f_{in}=200MHz	25°C		68.3		dBFS
Effective Number of Bits (ENOB)					
f_{in}=30.5MHz	25°C		11.8		Bits
f_{in}=70MHz	25°C		11.6		Bits
	Full	11.4			Bits
f_{in}=140MHz	25°C		11.1		Bits
f_{in}=200MHz	25°C		11.1		Bits
Spurious-free Dynamic Range (Third Harmonic)					
f_{in}=30.5MHz	25°C		87		dBc
f_{in}=70MHz	25°C		80		dBc
	Full	77			dBc
f_{in}=140MHz	25°C		80.1		dBc
f_{in}=200MHz	25°C		78		dBc
Spurious-free Dynamic Range (Second Harmonic)					
f_{in}=30.5MHz	25°C		81.6		dBc
f_{in}=70MHz	25°C		83		dBc
	Full	80			dBc
f_{in}=140MHz	25°C		78.6		dBc
f_{in}=200MHz	25°C		65		dBc
Crosstalk[1]	Full		-82		dB
Analog Input Bandwidth	25°C		650		MHz

1. Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 125MSPS sampling rate, VIN = -1.0 dBFS, 1.0 V internal reference, unless otherwise noted.

Table 3. Digital Specifications Parameter

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Differential Clock Inputs (CLK+/-)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common Mode Bias			0.9		V
Differential Input Voltage	Full	0.3		3.6	V
Input Voltage Range	Full	0		1.8	V
Input Resistance	Full		15		kΩ
Input Capacitance	Full		3.5		pF
LOGIC INPUTS (PDWN,SYNC,SCLK,CSB,SDIO)					
Logic 1 Voltage	Full	1.2		AVDD	V
Logic 0 Voltage	Full	0		0.6	V
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
DIGITAL OUTPUTS (D0±x, D1±x) ANSI-644					
Differential Output Voltage	Full	290	345	400	mV
Output Common-Mode Voltage	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

TIMING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 110MSps sampling rate, VIN = -1.0 dBFS, 1.0 V internal reference, unless otherwise noted.

Table 4. Switching Parameter

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
CLOCK					
Input Clock Rate	Full			880	MHz
Conversion Rate				110	MHz
Aperture Delay (t_A)	Full		1		ns
Aperture Uncertainty	Full		0.14		ps rms
OUTPUT PARAMETERS					
t_A	Full		1		ns
t_{EH}	Full		6.25/5/4.55		ns
t_{EL}	Full		6.25/5/4.55		ns
t_{CPD}	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
t_{FCO}	Full	1.5	2.3	3.1	ns
t_{FRAME}	Full	(t_{SAMPLE}/16)−300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16)+300	ps

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
t_{PD}	Full	1.5	2.3	3.1	ns
t_{DATA}	Full	(t_{SAMPLE}/16)−300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16)+300	ps
t_{LD}	Full		90		ps

NOTES: t_{SAMPLE} = 1/f

Timing Diagrams

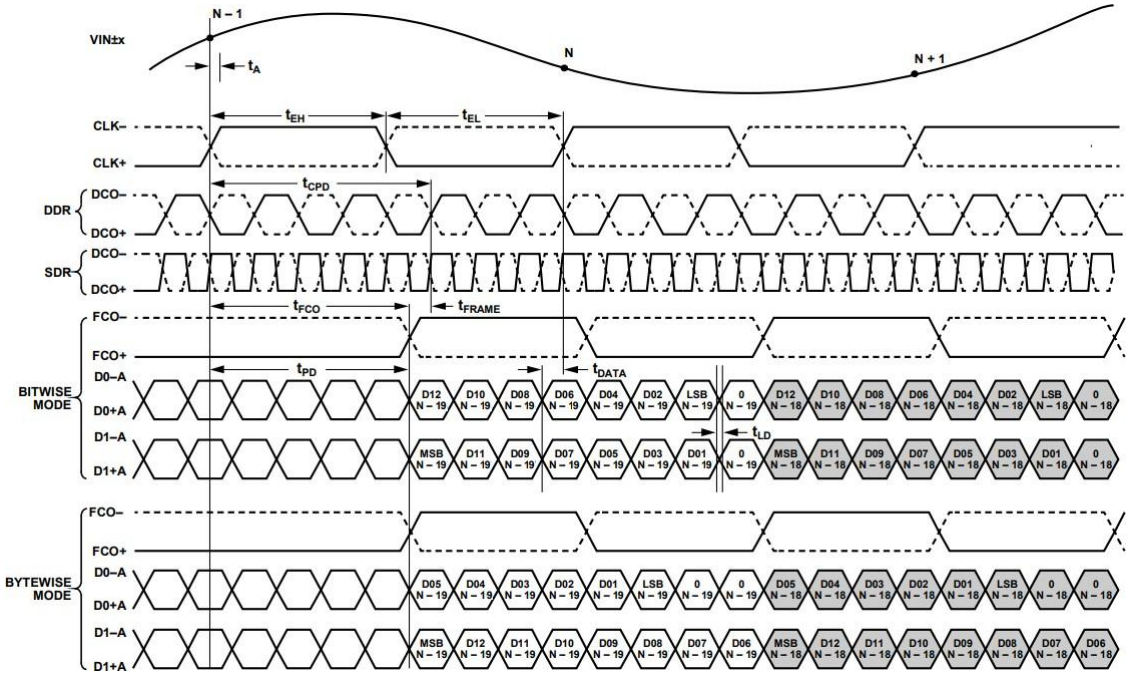


Figure 2. 16-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)

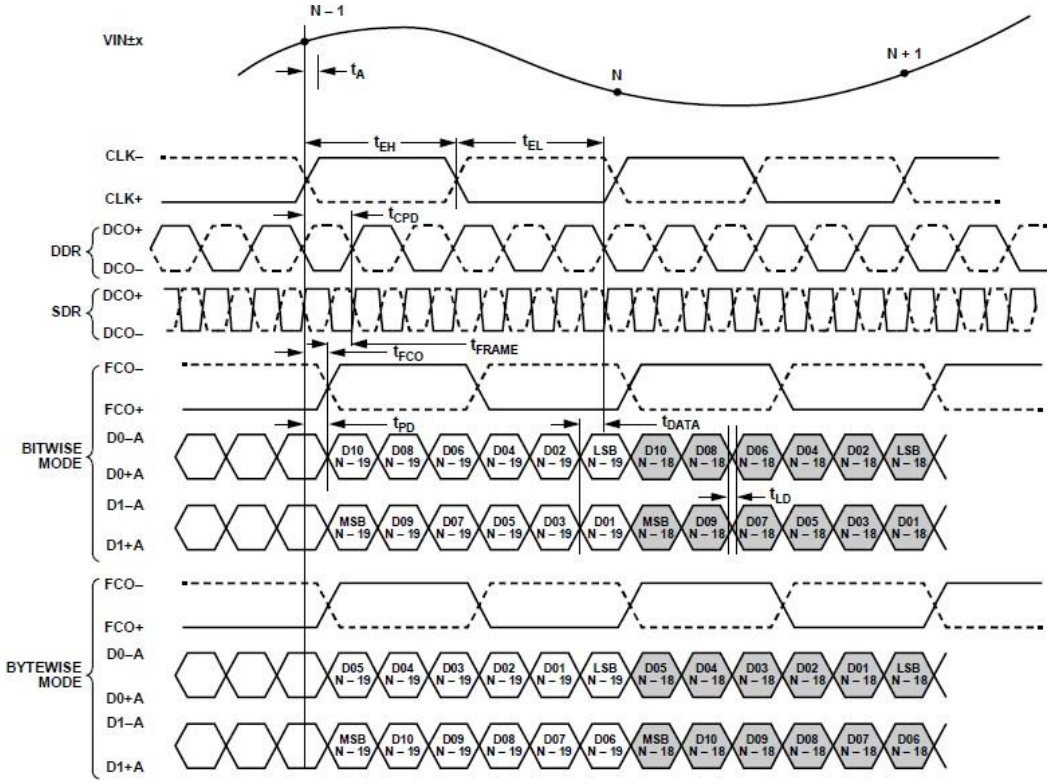


Figure 3. 12-Bit DDR/SDR, Two-Lane, 1× Frame Mode

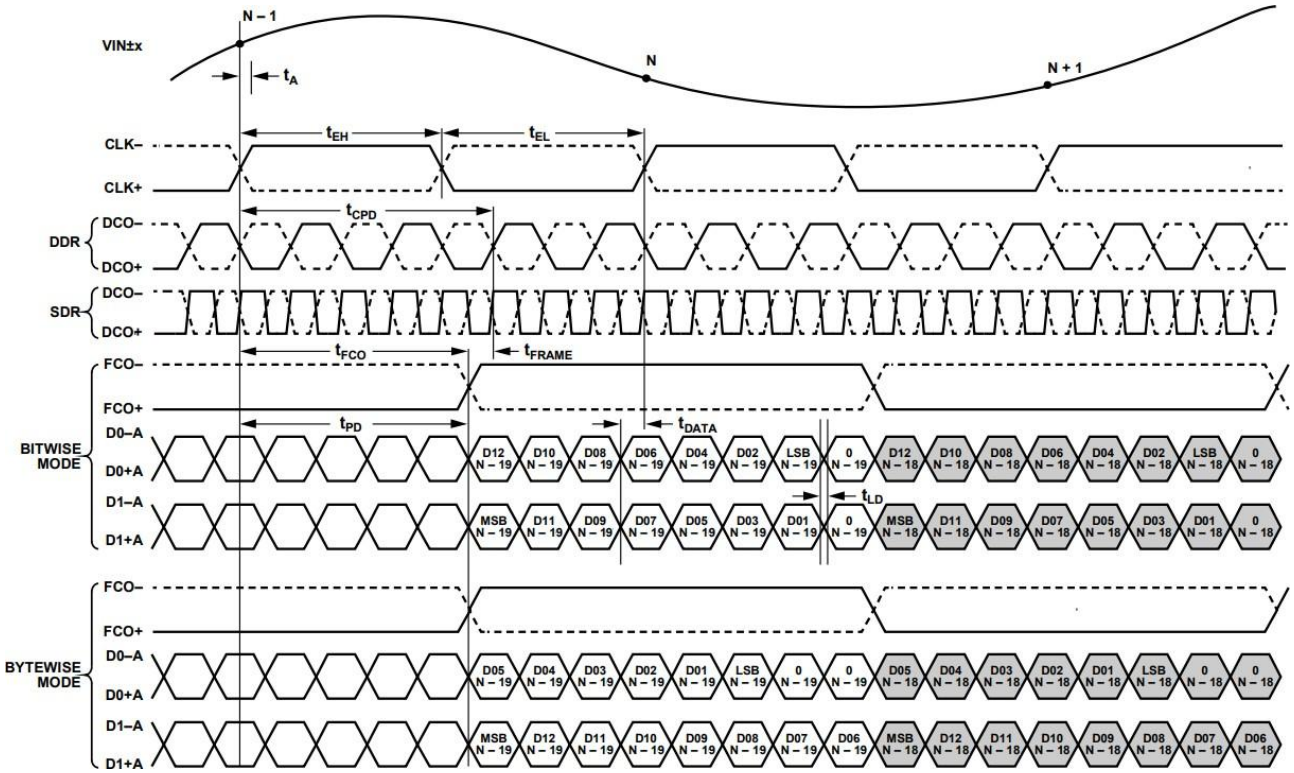


Figure 4. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode

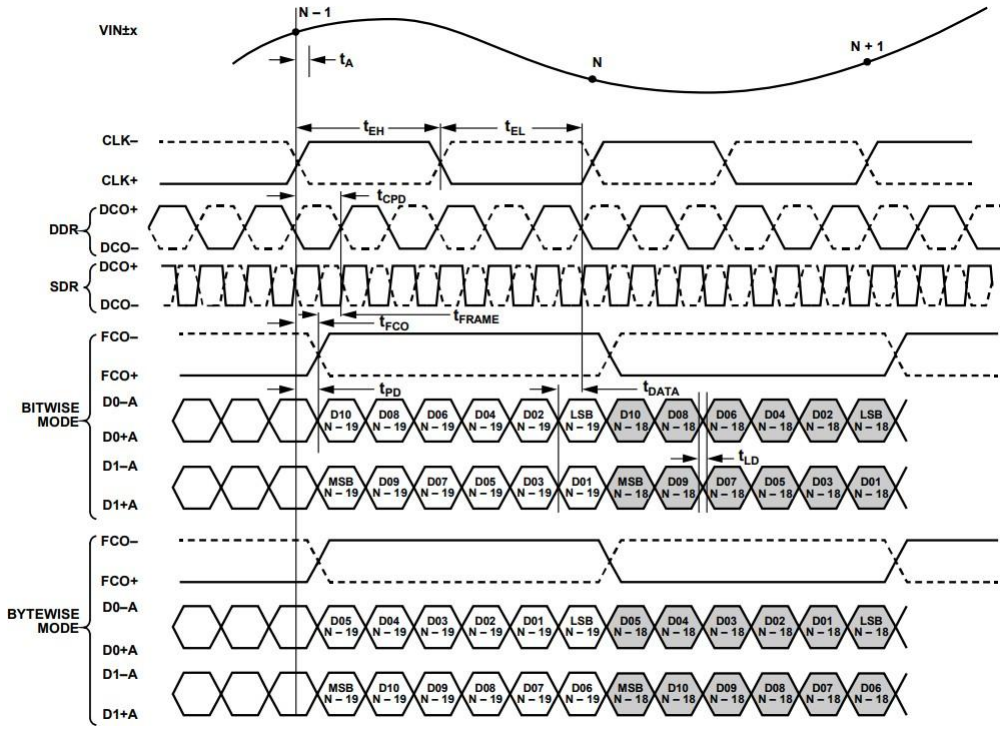


Figure 5. 12-Bit DDR/SDR, Two-Lane, 2× Frame Mode

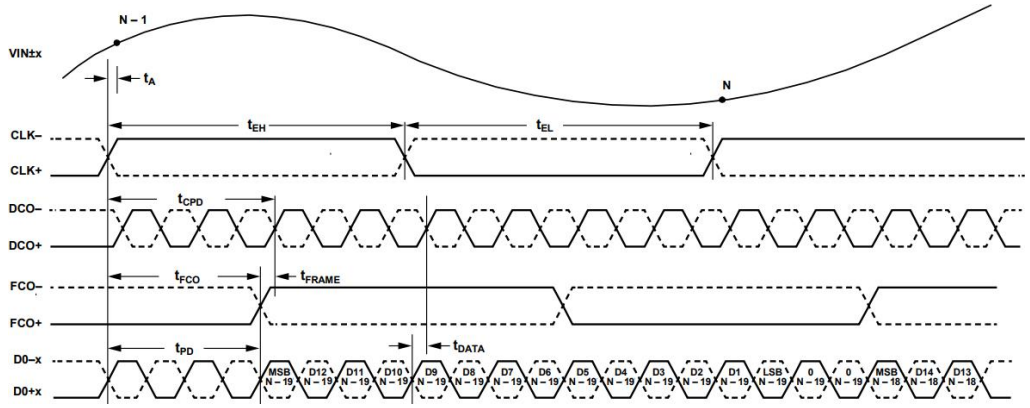


Figure 6. 16-Bit DDR, One-Lane, 1× Frame

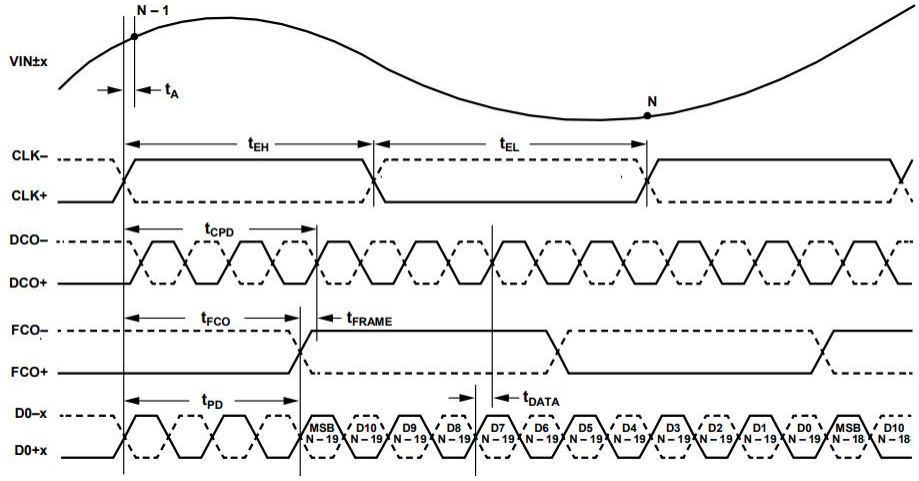


Figure 7. 12-Bit DDR, One-Lane, 1× Frame

Table 5. SPI Timing Parameter

PARAMETER	CONDITION	LIMIT
t_{DS}	Setup time between the data and the rising edge of SCLK	2ns, min
t_{DH}	Hold time between the data and the rising edge of SCLK	2ns, min
t_{CLK}	Period of the SCLK	40ns, min
t_S	Setup time between CSB and SCLK	2ns, min
t_H	Hold time between CSB and SCLK	2ns, min
t_{HIGH}	SCLK pulse width high	10ns, min
t_{LOW}	SCLK pulse width low	10ns, min

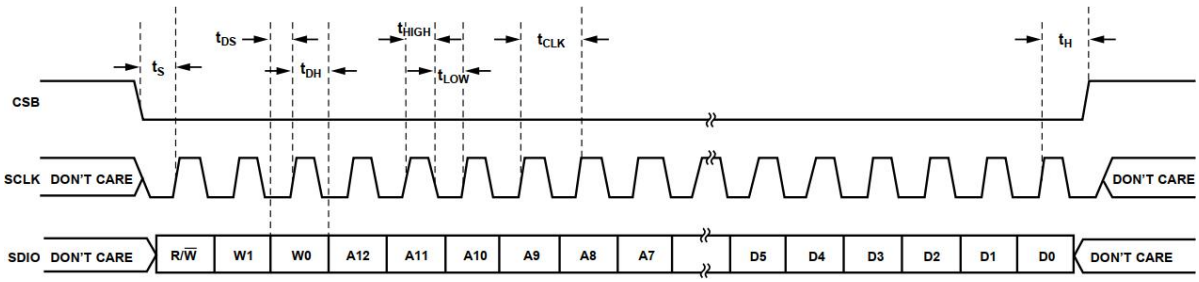


Figure 8. Serial Port Interface Timing

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (AVDD,DRVDD) to AGND ……-0.3V to 2V

Input Voltage (VIN+/-,CLK+/-,VREF,SENSE,VCM,RBIAS,CSB,SCLK,SDIO,PDWN) ...…-0.3V to 2V

Output Voltage (DCO, FCO, DxA/B/C/D)……..……-0.3V to 2V

Maximum Junction Temperature TJ,MAX……...……150°C

Operating Temperature Range……..……-40°C to 85°C

Storage Temperature Range……...… ……-65°C to 150°C

ESD(Human Body Model) ……...……2000V

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

ESD CAUTION

This product is an electrostatic sensitive device. Therefore, proper ESD precaution measures should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

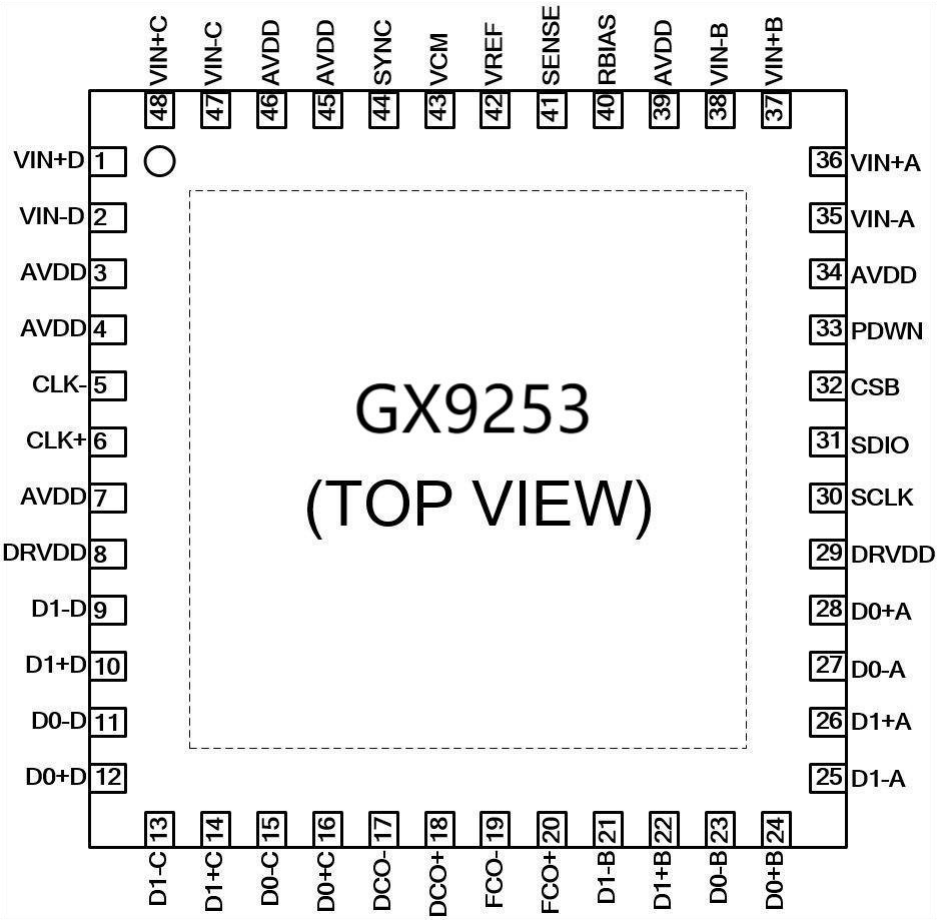


Figure 9. Pin (pad) Configuration

Table 6. Pin Definition

Pin No.	Pin Name	Pin Function
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation
1	VIN+D	Channel D Analog Input +
2	VIN−D	Channel D Analog Input -
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply
5, 6	CLK−, CLK+	Differential Clock Input
8, 29	DRVDD	Digital Output Driver Supply, 1.8V
9, 10	D1−D, D1+D	Channel D Digital Output
11, 12	D0−D, D0+D	Channel D Digital Output
13, 14	D1−C, D1+C	Channel D Digital Output
15, 16	D0−C, D0+C	Channel D Digital Output
17, 18	DCO−, DCO+	Data Clock Output
19, 20	FCO−, FCO+	Frame Clock Output

Pin No.	Pin Name	Pin Function
21, 22	D1−B, D1+B	Channel B Digital Output
23, 24	D0−B, D0+B	Channel B Digital Output
25, 26	D1−A, D1+A	Channel A Digital Output
27, 28	D0−A, D0+A	Channel A Digital Output
30	SCLK	SPI Clock Input
31	SDIO	SPI Data Input and Output
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down
		PDWN high = power-down device
		PDWN low = run device, normal operation
35	VIN−A	Channel A Analog Input -
36	VIN+A	Channel A Analog Input +
37	VIN+B	Channel B Analog Input +
38	VIN−B	Channel B Analog Input -
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground
41	SENSE	Reference Mode Selection
42	VREF	Voltage Reference Input and Output
43	VCM	Analog common mode input
44	SYNC	Digital Input. SYNC input to clock divider
47	VIN−C	Channel C Analog Input -
48	VIN+C	Channel C Analog Input +

TYPICAL CURVE

AVDD = 1.8 V, DRVDD = 1.8 V, TA=27ºC, 110MSPS sampling rate, VIN = -1.0 dBFS, 1.0 V internal reference, unless otherwise noted.

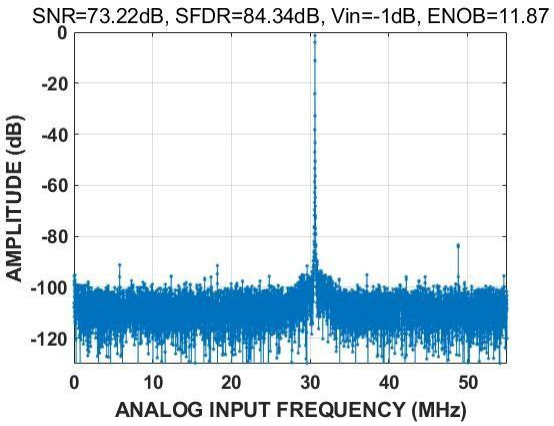


Figure 10. Tone FFT(fin = 30.5MHz@110MSPS)

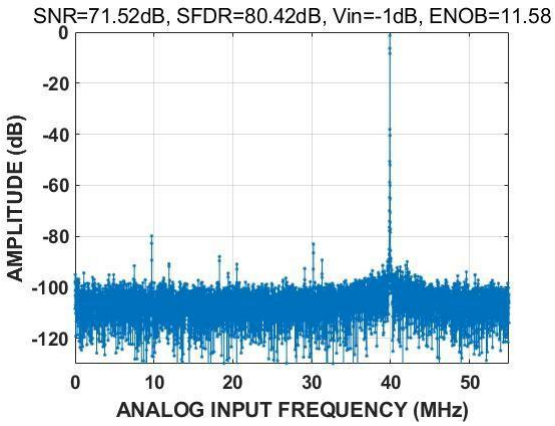


Figure 11. Tone FFT(fin = 70MHz@110MSPS)

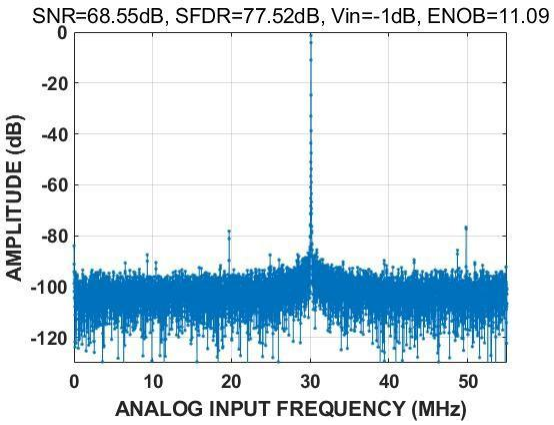


Figure 12. Tone FFT(fin = 140MHz@110MSPS)

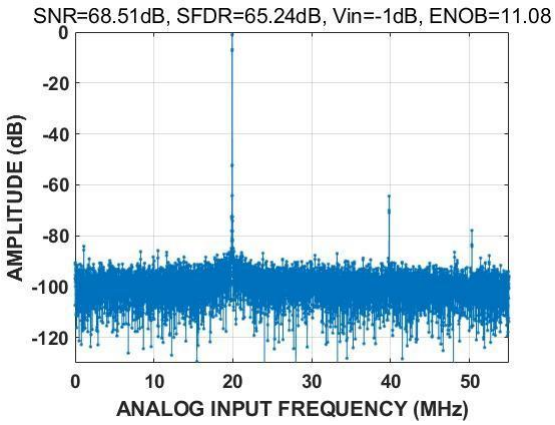


Figure 13. Tone FFT(fin = 200MHz@110MSPS)

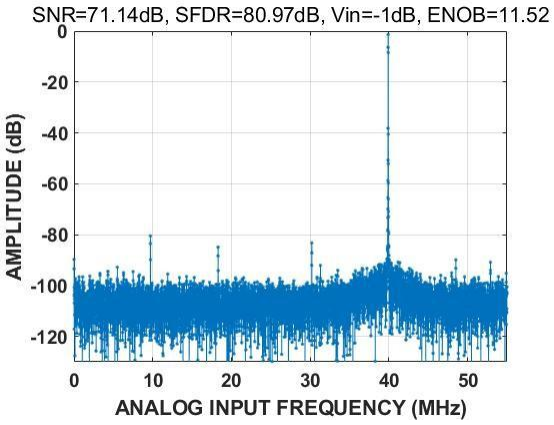


Figure 14. Tone FFT(fin = 70MHz@110MSPS) (-40℃)

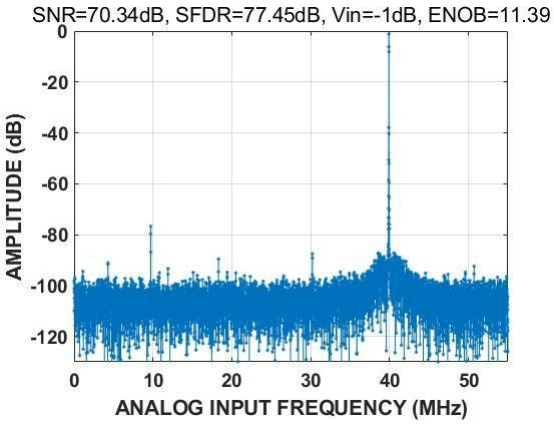


Figure 15. Tone FFT(fin = 70MHz@110MSPS) (+125℃)

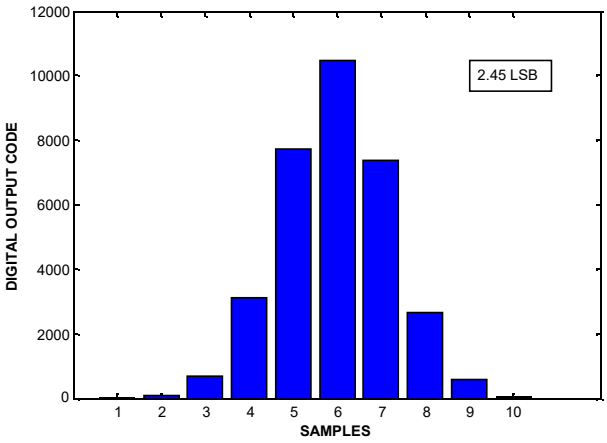


Figure 16. Input Grounding Histogram

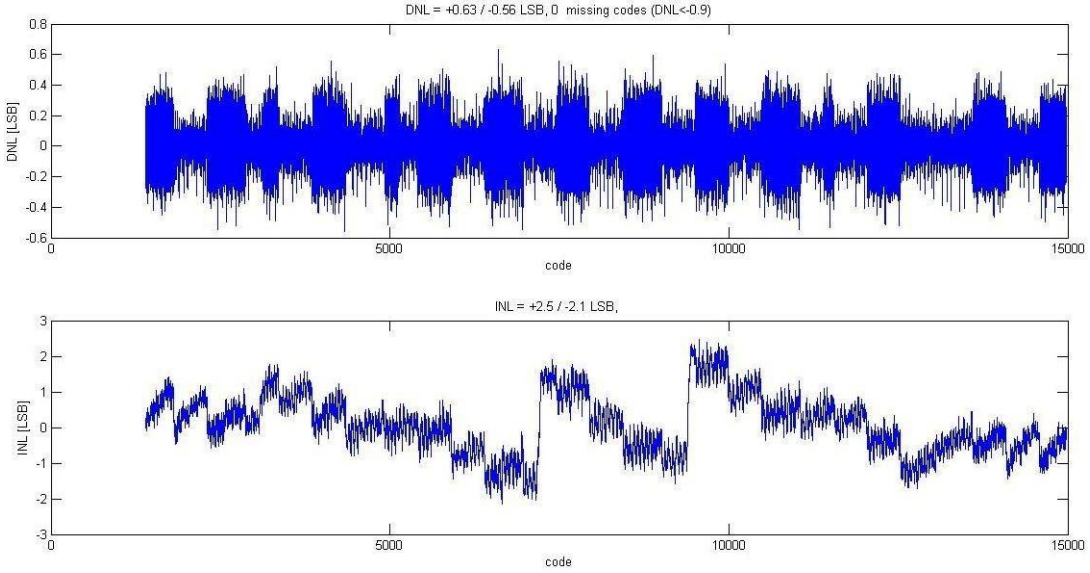


Figure 17. DNL/INL Difference

TYPICAL APPLICATION CIRCUIT

The typical application circuits of peripheral devices such as GX9253 input signal, input clock, and external DC pins are as follows.

ANALOG INPUT NETWORK

The optimal performance of ADC is achieved through differential driving of analog inputs. The use of differential double balun configuration to drive GX9253 provides excellent performance and flexible ADC interface for baseband applications (see Figure 18).

When the input frequency is in the second or higher Nyquist region, the noise performance of most amplifiers cannot meet the requirements to achieve the SNR of GX9253. Differential transformer coupling is the recommended input configuration (see Figure 19). Regardless of the configuration, the value of the parallel capacitor C1 depends on the input frequency and may need to be reduced or removed.

Using the input network method of VIN- connected to common mode voltage and VIN+ connected to input signal can cause the chip SNR to deteriorate, so it is not recommended to drive GX9253 input with a single end.

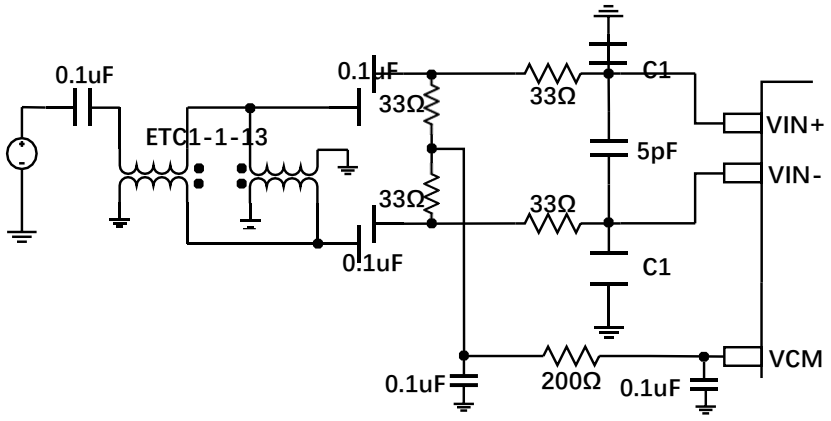


Figure 18. Differential Double Balun Input Configuration

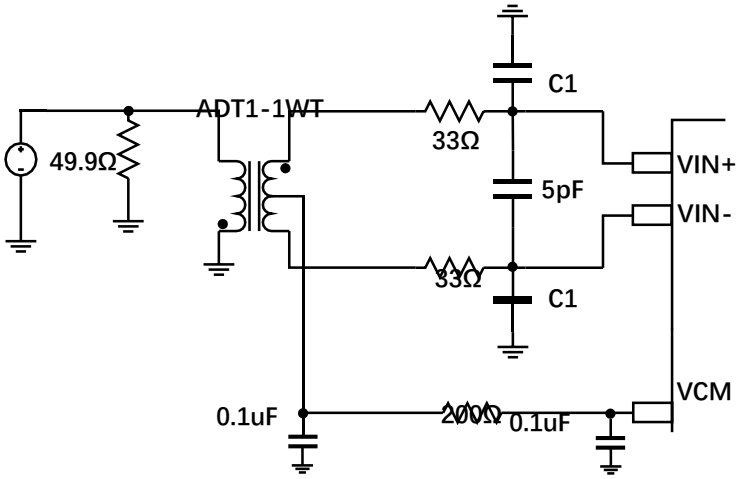


Figure 19. Differential Transformer-Coupled Input Configuration

CLOCK INPUT NETWORK

To fully utilize the performance of the chip, a differential signal should be used as the clock signal of the GX9253 sampling clock input (CLK+/-). The input clock pin has internal bias and does not require external bias. Suggest sampling the configuration of the RF transformer, as shown in Figure 20. The back-to-back Schottky diode connected to the transformer can limit the clock signal input to GX9253 to approximately 0.8V differential peak to peak. In this way, not only can the large voltage swing of the clock be prevented from feeding to other parts, but also the fast Rise and Fall time of the signal can be reserved, which is very important for low jitter performance.

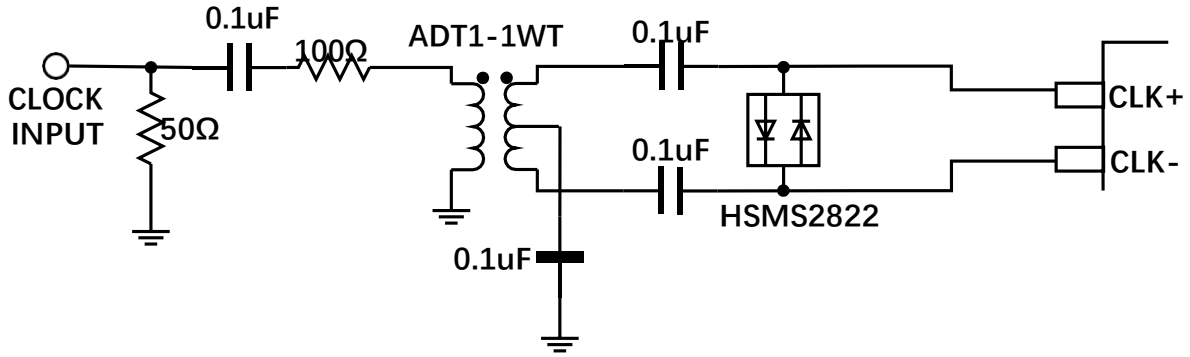


Figure 20. Clock Input

REFERENCE CONFIGURATION

A comparator within the GX9253 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 7. If SENSE pin is connected to ground, the reference amplifier switch is connected to the internal resistor divider, setting V_{REF} to 1.0 V. If the

internal reference of the GX9253 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. When the SENSE pin is connected to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference must be limited to a maximum of 1.0 V. It is not recommended to float the SENSE pin.

Table 7. Reference Voltage Summary

Mode	SENSE Voltage	Resulting V_{REF} (V)	Resulting Differential Span (V_{PP})
Fixed External Reference	AVDD	1.0	2.0
Fixed Internal Reference	AGND to 0.2	1.0	2.0

DIGITAL OUTPUTS FORMAT

The GX9253 output driver is a LVDS interface, and the timing is shown in Figure 2. The output driver should be able to provide sufficient output current to drive various logic circuits, and the driving force can be adjusted through registers. However, high driving current may cause spurious pulses in the power signal, affecting the performance of the converter. Therefore, in applications that require ADC to drive large capacity loads or large fanouts, external buffers or latches may be required. The default format of the output data is binary complement, and an example of the output encoding format is shown in Table 8. The format of the output data can also be modified through registers.

Table 8. Digital Output Coding

Input (V)	Condition	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN-	< –VREF – 0.5LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ – VIN-	= –VREF	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ – VIN-	= 0	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ – VIN-	= +VREF – 1LSB	1111 1111 1111 1100	0111 1111 1111 1100
VIN+ – VIN-	> +VREF – 0.5LSB	1111 1111 1111 1100	0111 1111 1111 1100

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to one data cycle (30° relative to one DCO cycle). This enables the user to refine system timing margins if required. The default DCO± to output data edge timing, as shown in Figure 2, is 180° relative to one data cycle (90° relative to one DCO cycle). In default mode, the MSB is first in the data output serial stream. This can be inverted so that the LSB is first in the data output serial stream by using the SPI.

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 9 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. Note that some patterns do not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T0.150 (05/96) standard. The initial values are all 1s (see Table 10). The output is a parallel

representation of the serial PN9 sequence in MSB-first format. The first output word is the first 14 bits of the PN9 sequence in MSB aligned form.

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8388607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T0.150 (05/96) standard. The initial values are all 1s (see Table 10), GX9253 Inverts Bitstream According to ITU Standards. The output is a parallel representation of the serial PN23 sequence in MSB-first format. The first output word is the first 14 bits of the PN23 sequence in MSB aligned form.

Table 9. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0000	Off (default)	N/A	N/A	N/A	
0001	Midscale short	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	N/A	Yes	Offset binary code shown
0010	+Full-scale short	1111 1111 1111 (12-bit) 1111 1111 1111 1111(16-bit)	N/A	Yes	Offset binary code shown
0011	−Full-scale short	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	N/A	Yes	Offset binary code shown
0100	Checkerboard	1010 1010 1010 (12-bit) 1010 1010 1010 1010 (16-bit)	0101 0101 0101 (12-bit) 0101 0101 0101 0101 (16-bit)	No	
0101	PN sequence long	N/A	N/A	Yes	PN23 ITU 0.150 $X^{23}+ X^{18}+1$
0110	PN sequence short	N/A	N/A	Yes	PN9 ITU 0.150 $X^{9}+ X^{5}+1$
0111	One-/zero-word Toggle	1111 1111 1111 (12-bit) 111 1111 1111 1100 (16-bit)	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	No	
1000	User input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No	
1001	1-/0-bit toggle	1010 1010 1010 (12-bit)	N/A	No	
1010	1× sync	1010 1010 1010 1000 (16-bit) 0000 0011 1111 (12-bit)	N/A	No	
1011	One bit high	0000 0001 1111 1100 (16-bit) 1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	N/A	No	Pattern associated with the external pin
1100	Mixed frequency	1010 0011 0011 (12-bit) 1010 0001 1001 1100 (16-bit)	N/A	No	

Table 10. PN Sequence

Sequence	Initial Value	Next Three Output Samples (MSB First) Twos Complement
PN Sequence Short	0x1FE0	0x1DF1, 0x3CC8, 0x294E
PN Sequence Long	0x1FFF	0x1FE0, 0x2001, 0x1C00

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

CSB PIN

The CSB pin must be tied to AVDD for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored.

RBIAS PIN

To set the internal core bias current of the ADC, place a 10.0 kΩ, 1% tolerance resistor to ground at the RBIAS pin.

OUTPUT TEST MODES

The output test options are described in Table 9 and controlled by the output test mode bits at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block.

Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock.

SERIAL PORT INTERFACE (SPI)

The GX9253 Serial Port Interface (SPI) allows users to configure the corresponding function registers inside the ADC to meet specific functional and operational needs. Through the serial port, the address space can be accessed and read and written. Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 15). The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles. The timing requirements are shown in Figure 8.

MEMORY MAP REGISTER TABLE

Table 12. Memory Map Register Table

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
0x00	SPI port configuration	0 =SDO active	LSB first	Soft reset	1 =16-bit address	1 =16-bit address	Soft reset	LSB first	0 =SDO active	0x18	The default for ADCs is 16-bit mode.
0x01	Chip ID	0x8F = quad 14-bit 80 MSPS/100 MSPS/110 MSPS serial LVDS								0x8F	Unique chip ID used to differentiate devices; read only.
0x02	Chip grade		100 = 80 MSPS 101 = 100 MSPS 110 = 110 MSPS								Unique speed grade ID used to differentiate graded devices; read only.
0x05	Channel select			Clock Channel DCO	Clock Channel FCO	Data Channel D	Data Channel C	Data Channel B	Data Channel A	0x3F	Determines which device on chip receives the

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
											next write command. The default is all devices on chip
0x08	Mode			External pin function 0x00 full power-down 0x01 standby				00 = chip run 01 = full power-down 10 = standby 11 = digital reset		0x00	Determines various generic modes of chip operation.
0x0B	Clock divide						Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 1 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 5 110 = divide by 6 111 = divide by 7			0x00	
0x0D	Test mode	User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once		Reset PN long sequence	Reset PN short sequence	Output test mode:0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1x sync 1011 = one bit high 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output pins in place of normal data.

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
0x10	Offset adjust	8-bit device offset adjustment [7:0] Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Device offset trim
0x14	ADC Output mode		LVDS-ANSI/LVDS-IEEE option 0=LVDSANSI 1=LVDSIEEE reduced range link				Output Invert		Output format 0 = offset binary 1 = two's complement	0x01	Configures the outputs and the format of the data.
0x19	USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern, 1 LSB
0x1A	USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern, 1 MSB
0x1B	USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern, 2 LSB
0x1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern, 2 MSB

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
0x21	Serial output data control	LVDS output LSB first	SDR/DDR one-lane/two-lane, bitwise/bytewise[6:4] 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise 100 = DDR one-lane				Select 2x frame		output number of bits 00 = 16 bits 10 = 12 bits	0x30	Serial stream control
0x22	Serial channel status							Channel output reset	Channel Power-down	0x00	Used to power down individual sections of a converter.
0x33	Serial output phase adjustment	FCO delay phase select			DCO delay phase select			[1]:invert FCO [0]:invert DCO Valid when 0x14[2] = 1'b0		0x00	Used to adjust the phase delay between DCO and FCO
0x34	Serial output adjustment			FCO Clock LVDS Load Select 3'b000: External R 3'b001: R=200 3'b010: R=100 3'b011: R=66.7 3'b100: R=50 3'b101: R=40 3'b110: R=33.3 3'b111: R=28.5		DCO Clock LVDS Load Select 3'b000: External R 3'b001: R=200 3'b010: R=100 3'b011: R=66.7 3'b100: R=50 3'b101: R=40 3'b110: R=33.3 3'b111: R=28.5			0x00	Determines LVDS or other output attributes
0x35	Serial output adjustment					12/16bit 1x FCO: 4'd1 16bit 2x FCO: 4'd5 12bit 2x FCO: 4'd4 frame clock phase shift 4'b0000:no shift 4'b0001:shift one clock period ……				0x01	FCO clock adjustment

ADDR (HEX)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value (HEX)	Comments
0x41	Serial output adjustment	[7]:invert D1 LVDS [6]:invert D0 LVDS Valid when 0x14[2] = 1'b0;		For D1 LVDS 3'b000: External R 3'b001: R=200 3'b010: R=100 3'b011: R=66.7 3'b100: R=50 3'b101: R=40 3'b110: R=33.3 3'b111: R=28.5			For D0 LVDS 3'b000: External R 3'b001: R=200 3'b010: R=100 3'b011: R=66.7 3'b100: R=50 3'b101: R=40 3'b110: R=33.3 3'b111: R=28.5			0x00	Determines LVDS or other output attributes
0x42	Serial output phase adjustment			D1 delay phase select			D0 delay phase select			0x00	Used to adjust the phase delay between D0 and D1
0x102	I/O Control					VCM Power-down				0x00	VCM Control
0x109	SYNC							SYNC only first pulse	SYNC enable	0x00	

APPLICATION INFORMATION

POWER AND GROUND RECOMMENDATIONS

It is recommended that two separate power supplies are used for the GX9253. one is for analog power (AVDD),the other is for digital power (DRVDD). For AVDD and DRVDD, several different decoupling capacitors should be used to reduce high and low frequencies noise. these capacitors should be close to the pins of the device with minimal trace length. A single PCB ground plane is sufficient for the GX9253. With proper decoupling and being isolated between sections of analog, digital, and clock, optimum performance is easily achieved.

EXPOSED PAD RECOMMENDATIONS

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. continuous exposed (no solder mask) copper plane on the PCB should match the GX9253 exposed paddle. The copper plane should have as much as through vias to achieve as lower as thermal resistance for heat dissipation.

These vias should be filled to prevent solder wicking. To optimized adhere the ADC to the PCB, silkscreen is recommended to partition the continuous plane on the PCB into several uniform sections that provide several tie points between the ADC and the PCB during the reflow process. Since there is only one connection point between the ADC and the PCB Using one continuous plane with no partitions.

VCM

The VCM pin should be decoupled to ground with a 0.1 μF capacitor.

REFERENCE DECOUPLING

The V_{REF} pin must be externally decoupled to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

SPI PORT

The SPI port must not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the GX9253 to keep these signals from transitioning at the converter inputs during critical sampling periods.

DATA OUTPUT

Due to circuit structure issues, if there is a requirement for a fixed data output delay, there is a power on timing requirement, that is, first power on the DRVDD's power then wait a few milliseconds before powering on the AVDD and program as follows:

SPI_Write (0x3D 0x20);

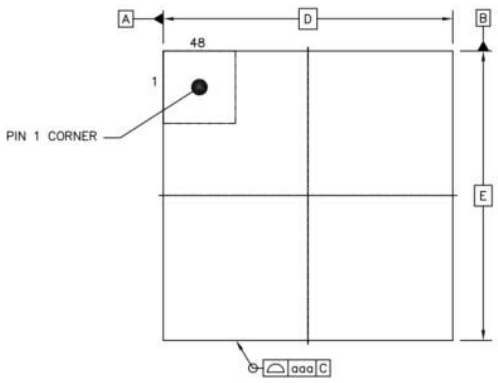
SPI_Write (0x3D 0x00);

If data synchronization output between channels is required, the data output path needs to be reset as follows:

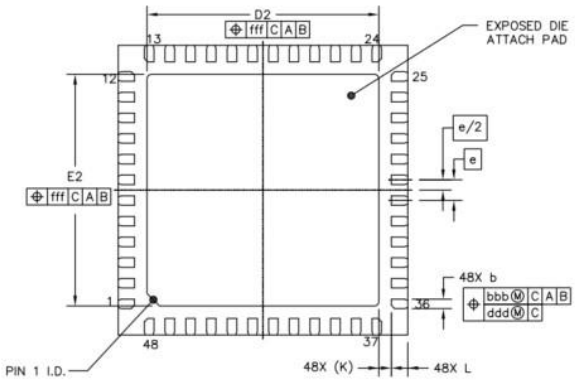
SPI_Write (0x08 0x03);

SPI_Write (0x08 0x00);

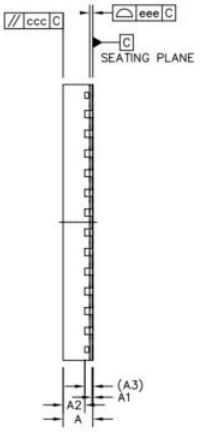
OUTLINE DIMENSION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5.5	5.6	5.7
	Y	E2	5.5	5.6	5.7
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Figure 21. 48 Pin QFN (Dimension shown in millimeter)

ORDERING GUIDE

Table 13. Order Information

Part No.	Temperature Range	Package
GX9253GDLUCY-80	-40 ~ 85℃	QFN-48
GX9253GDLUCY-105	-40 ~ 85℃	QFN-48
GX9253GDLUCY-125	-40 ~ 85℃	QFN-48

Customed packages are available

DECLARATION

The information above is for reference only and is intended to assist GXSC (Shenzhen) Technology Co., Ltd customers in their design and development. GXSC (Shenzhen) Technology Co., Ltd reserves the right to change the above information without prior notice due to technological innovation.

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