# GX9268 16-Bit 80/105MSPS Dual ADC

## FATURES

- 1.8V analog supply
- 1.8V digital output supply
- Low power：
  485mW (105MSPS)
- SNR=77.2dBFS（fin=30.5MHz@105MSPS）
- SFDR=88dBc（fin=30.5MHz@105MSPS）
- On-chip reference voltage and sample-and-hold circuits.
- QFN-64 package 9mm×9mm

## APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
- I/Q demodulation systems
- Smart antenna systems
- Battery powered instruments
- Handheld oscilloscope
- Portable medical imaging
- Ultrasound equipment
- Radar/LIDAR

## FUNCTIONAL BLOCK DIAGRAM

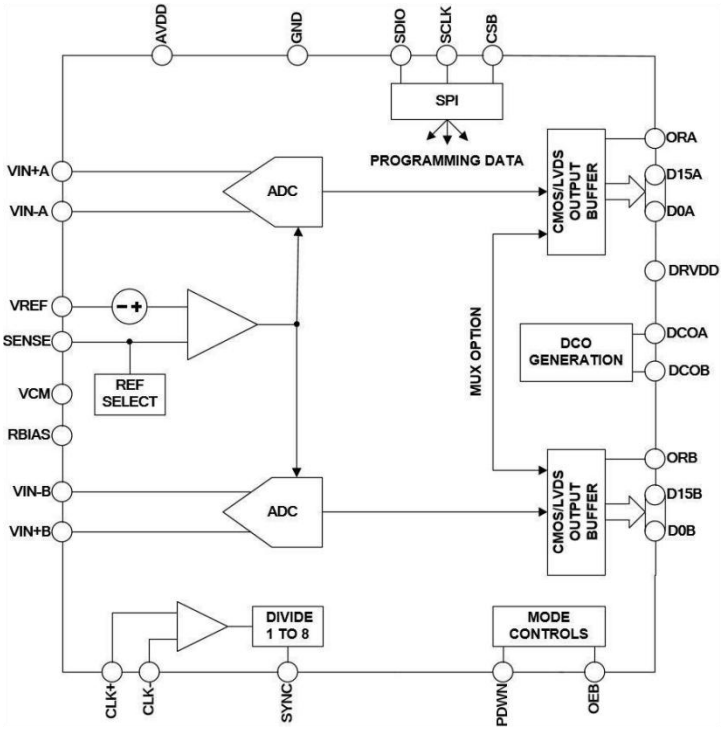


Figure 1 Functional Block Diagram

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## GENERAL DESCRIPTION

The GX9268 is a single-chip, dual-channel, 14-bit, 80 MSPS/105 MSPS analog-to-digital converter (ADC). The GX9268 is powered by a 1.8V power supply, equipped with a high-performance sample-and-hold circuit and an on-chip reference voltage.

The GX9268 features a multistage, differential pipelined architecture with integrated output error correction logic. It provides 16 bits accuracy at a data rate of 105MSPS and ensures no code loss throughout the entire operating temperature range. The ADC is equipped with multiple built-in functional features, which can maximize the flexibility of the device and minimize the system cost, such as generating programmable digital test codes, etc. The available digital test codes include built-in fixed code and pseudo-random code, as well as user-defined test codes input through the Serial Port Interface (SPI).

A differential clock input can be used to control all internal conversion cycles. The digital output data format can be offset binary, gray code or binary complement. Each ADC channel has a data output clock (DCO) to ensure that the receiving logic has the correct latch timing. This device supports 1.8V CMOS output and LVDS output, and the output data can be multiplexed on a single output bus.

The GX9268 is available in a 64-lead QFN package and is specified over the RoHS standard.

# SPECIFICATIONS

## ADC DC Specifications

AVDD=1.8 V、DRVDD=1.8 V、VIN=−1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 1 ADC DC Specifications

| Parameter | Temp | GX9268-80 | | | GX9268-105 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Resolution | | | 16 | | | 16 | | Bits |
| No Missing Codes | Full | | Guaranteed | | | Guaranteed | | |
| Offset Error | Full | | ±0.1 | ±0.7 | | ±0.1 | ±0.7 | %FSR |
| Gain Error | Full | | -1.5 | | | -1.5 | | %FSR |
| Differential Nonlinearity [1](DNL) | Full<br>25℃ | -0.75 | <br>±0.45 | 0.75 | -0.75 | <br>±0.45 | 0.75 | LSB<br>LSB |
| Integral Nonlinearity[1](INL) | Full<br>25℃ | -2.5 | <br>±1.0 | 2.5 | -2.5 | <br>±1.0 | 2.5 | LSB<br>LSB |
| Internal Voltage Reference Error | Full | | ±5 | | | ±5 | | mV |
| Input Reference Noise (VREF=1V) | 25℃ | | 0.98 | | | 0.98 | | LSB rms |
| Analog Input Span (VREF=1V) | Full | | 2 | | | 2 | | Vpp |
| Input Capacitance [2] | Full | | 4 | | | 4 | | pF |
| Input Common-Mode Voltage | Full | | 0.95 | | | 0.95 | | V |
| AVDD Supply Voltage | Full | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| DRVDD Supply Voltage | Full | 1.7 | | 1.8 | 1.7 | | 1.8 | V |
| $I_{AVDD}$ Supply Current | Full | | 194.9 | 200 | | 200.8 | 210 | mA |
| $I_{DRVDD1}$ Supply Current (CMOS)<br>$I_{DRVDD2}$ Supply Current (LVDS) | Full<br>Full | | 76.2<br>66.9 | | | 81<br>69.7 | | mA<br>mA |
| DC Input Power Consumption | 25℃ | | 475 | 490 | | 485 | 500 | mW |
| Sine Wave Input Power Consumption [1](CMOS)<br>Sine Wave Input Power Consumption [1](LVDS) | Full<br>Full | | 488<br>471 | | | 507<br>487 | | mW<br>mW |
| Power-Down Power | 25℃ | | 2 | | | 2 | | mW |

1. Measured with a 5MHz input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
2. Input capacitance refers to the effective capacitance between one differential input pin and AGND.

## ADC AC Specifications

AVDD=1.8 V、DRVDD=1.8 V、VIN=−1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 2 ADC AC Specifications

| Parameter | Temp | GX9268-80 | | | GX9268-105 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Signal-To-Noise Ratio (SNR) | | | | | | | | |
| $f_{in}$=30.5MHz | 25℃ | | 78.7 | | | 77.2 | | dBFS |
| | Full | 78.2 | | | 76.8 | | | dBFS |
| $f_{in}$=60MHz | 25℃ | | 77.6 | | | 76.5 | | dBFS |
| Signal-To-Noise and Distortion (SNDR) | | | | | | | | |
| $f_{in}$=30.5MHz | 25℃ | | 77.7 | | | 76.9 | | dBFS |
| | Full | 77.2 | | | 76.5 | | | dBFS |
| $f_{in}$=60MHz | 25℃ | | 76.1 | | | 74.4 | | dBFS |
| Effective Number of Bits (ENOB) | | | | | | | | |
| $f_{in}$=30.5MHz | 25℃ | | 12.6 | | | 12.5 | | Bit |
| | Full | 12.5 | | | 12.4 | | | Bit |
| $f_{in}$=60MHz | 25℃ | | 12.3 | | | 12.1 | | Bit |
| Spurious-Free Dynamic Range (Third Harmonic) | | | | | | | | |
| $f_{in}$=30.5MHz | 25℃ | | 92 | | | 92 | | dBc |
| | Full | 88 | | | 88 | | | dBc |
| $f_{in}$=60MHz | 25℃ | | 82 | | | 82 | | dBc |
| Spurious-Free Dynamic Range (Second Harmonic) | | | | | | | | |
| $f_{in}$=30.5MHz | 25℃ | | 93 | | | 93 | | dBc |
| | Full | 87 | | | 87 | | | dBc |
| $f_{in}$=60MHz | 25℃ | | 95 | | | 85 | | dBc |
| Crosstalk [1] | Full | | -92 | | | -92 | | dB |
| Analog Input Bandwidth | 25℃ | | 700 | | | 700 | | MHz |

1、Crosstalk is measured at 60 MHz with −1.0 dBFS on one channel and no input on the alternate channel.

## Digital Specifications

AVDD=1.8 V、DRVDD=1.8 V、VIN=−1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 3 Digital Specification Parameter

| Parameter | Temp | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Differential Clock Inputs（CLK+/-） | | | | | |
| Logic Compliance | Full | | CMOS/LVDS/LVPECL | | |
| Internal Common-Mode Bias | Full | | 0.9 | | V |
| Differential Input Voltage | Full | 0.2 | | 3.6 | V |
| Input Voltage Range | Full | GND-0.3 | | AVDD+0.2 | V |
| Input Resistance | Full | | 8 | | kΩ |
| Input Capacitance | Full | | 3.5 | | pF |
| Logic Input （PDWN,SYNC,SCLK,CSB,SDIO） | | | | | |
| High Level Input Voltage | Full | 1.2 | | DRVDD+0.3 | V |
| Low Level Input Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | Full | | 26 | | kΩ |
| Input Capacitance | Full | | 2 | | pF |
| Digital Output DRVDD = 1.8V | | | | | |
| High Level Input Voltage | Full | 1.79 | | | V |
| Low Level Input Voltage | Full | | | 0.2 | V |
| Code Mode（Default） | | | Offset Binary | | |

## Timing Specifications

AVDD=1.8 V、DRVDD=1.8 V、VIN=−1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 4 Timing Specifications

| Parameter | Temp | GX9268-80 | | | GX9268-105 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Clock Parameters | | | | | | | | |
| Input Clock Rate | Full | | | 625 | | | 625 | MHz |
| Conversion Rate | Full | | | 80 | | | 105 | MHz |
| Aperture Delay ($t_A$) | Full | | 1 | | | 1 | | ns |
| Aperture Jitter | Full | | 0.1 | | | 0.1 | | ps rms |
| Data Output Parameters | | | | | | | | |
| $t_A$ | Full | | 1 | | | 1 | | ns |
| $t_{CH}$ | Full | | 6.25 | | | 4.76 | | ns |
| $t_{CLK}$ | Full | | 12.5 | | | 9.52 | | ns |
| $t_{DCO}$ | Full | | 3 | | | 3 | | ns |
| $t_{PD}$ | Full | | 3 | | | 3 | | ns |
| $t_{SKEW}$ | Full | | 0.1 | | | 0.1 | | ns |

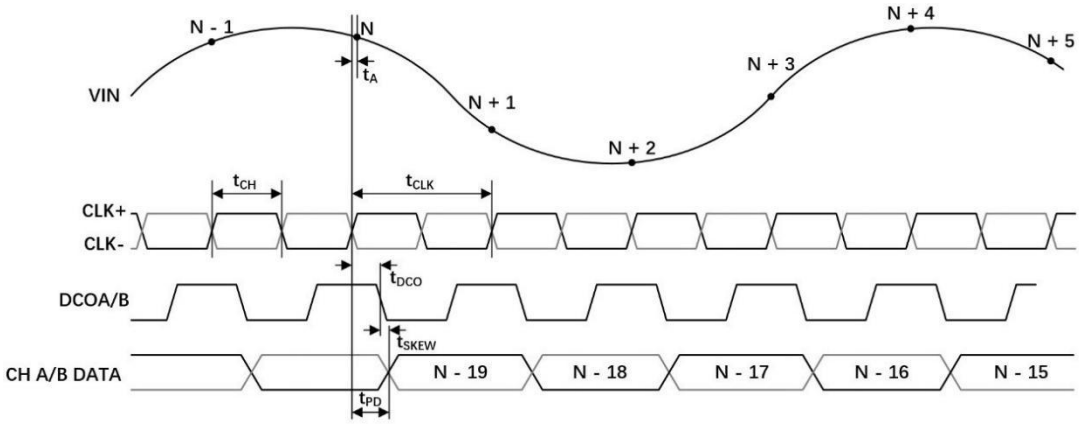



Figure 2 CMOS Output Timing

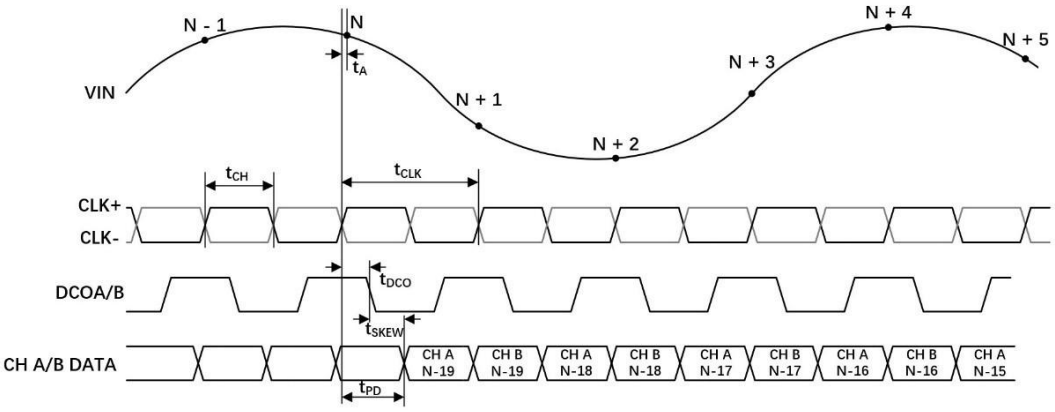



Figure 3 CMOS Interleaved Output Mode Data Output Timing (Output on Channel A Output Pin)

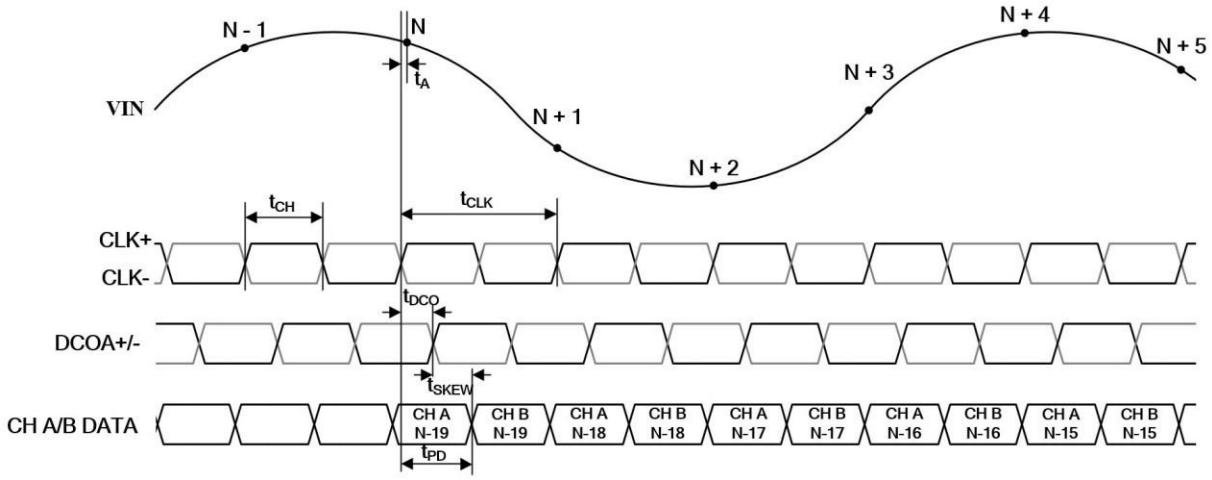



Figure 4 LVDS Output Timing

Table 5 SPI Timing Parameter

| Parameter | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|
| $t_{DS}$ | 2 | | | ns | Setup time between the data and the rising edge of SCLK |
| $t_{DH}$ | 2 | | | ns | Hold time between the data and the rising edge of SCLK |
| $t_{CLK}$ | 40 | | | ns | Period of the SCLK |
| $t_S$ | 2 | | | ns | Setup time between CSB and SCLK |
| $t_H$ | 2 | | | ns | Hold time between CSB and SCLK |
| $t_{HIGH}$ | 10 | | | ns | SCLK pulse width high |
| $t_{LOW}$ | 10 | | | ns | SCLK pulse width low |

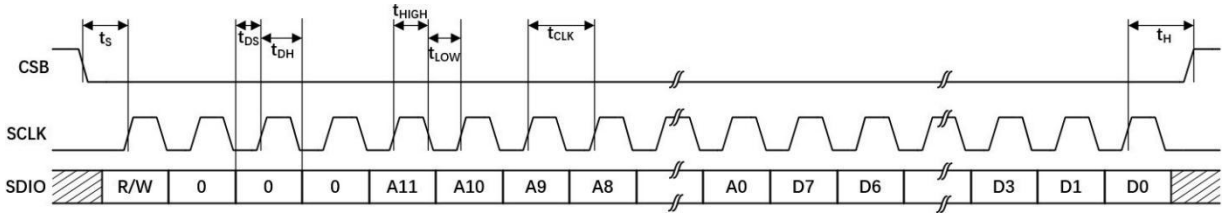



Figure 5 Serial Port Interface Timing

## ABSOLUTE MAXIMUM RATINGS

AVDD TO AGND……-0.3V to 2V

DRVDD TO AGND……..-0.3V to 3.9V

Input Voltage (VIN+/-, CLK+/-, VREF, SENSE, VCM, RBIAS)……-0.3V to AVDD+0.2V

Input Voltage (CSB, SCLK, SDIO, PDWN)……..-0.3V to DRVDD+0.3V

Output Voltage (DCOA,DCOB,D0A/D0B 至D13A/D13B)……-0.3V to DRVDD+0.3V

Maximum Junction Temperature $T_{J,MAX}$……150°C

Operating Temperature Range……-40°C to 85°C

Storage Temperature Range……...-65°C to 150°C

ESD (Human Body Model)……2000V

ATTENTION: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

## ESD CAUTION

This product is an electrostatic sensitive device. Therefore, proper ESD precaution measures should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

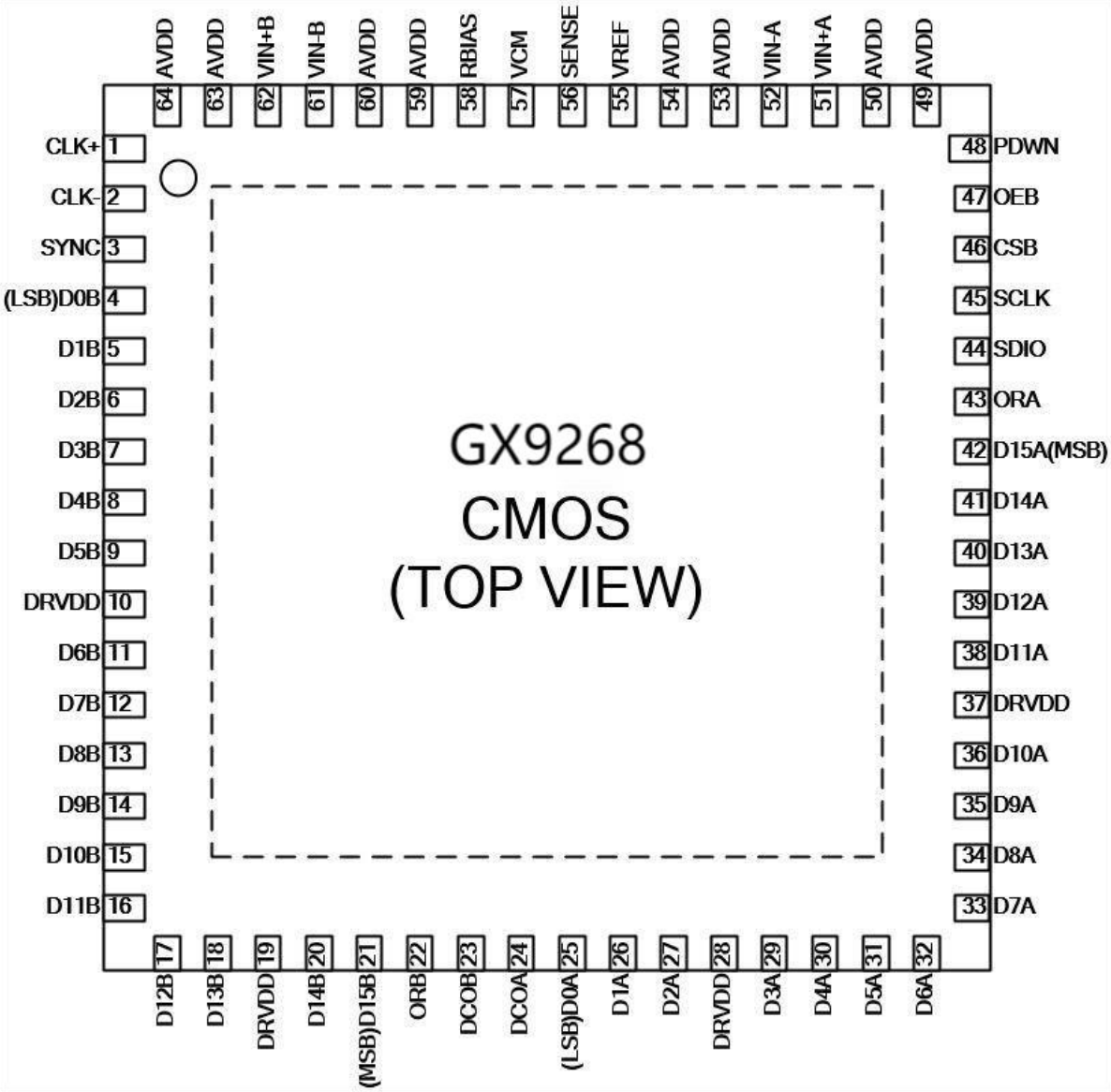



Figure 6 Pin Configuration

Table 6 Pin Function Description

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 0 | GND | G | Analog Ground. The pad on the bottom of the package provides the analog ground for the part. This bottom pad must be connected to ground for proper operation for ADC. |
| 1,2 | CLK−, CLK+ | AI | Differential Clock Input |
| 3 | SYNC | DI | Digital Input. Synchronous input clock divider |
| 4 to 9, 11 to 18, 20, 21 | D0B to D15B | DO | Channel B Output Data |
| 10, 19, 28, 37 | DRVDD | P | Digital Output Driver Supply. 1.8V Nominal |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 22 | ORB | DO | Channel B Output Data. Analog input overrange prompt pin |
| 23 | DCOB | DO | Channel B Data Clock Output |
| 24 | DCOA | DO | Channel A Data Clock Output |
| 25 to 27, 29 to 36, 38 to 42 | D0A to D15A | DO | Channel A Output Data |
| 43 | ORA | DO | Channel A Output Data. Analog input overrange prompt pin |
| 44 | SDIO | DIO | SPI Data I/O |
| 45 | SCLK | DI | SPI Clock Input |
| 46 | CSB | DI | SPI Chip Select. Active low, 30 kΩ internal pull-up |
| 47 | OEB | DI | Digital Input. If logic low, Channel A and Channel B output Data; if logic high, three-state output. 30kΩinternal pull-down. |
| 48 | PDWN | DI | Digital Input. 30kΩinternal pull-down.<br>PDWN high = power-down.<br>PDWN low = operation. |
| 49, 50, 53, 54, 59, 60, 63, 64 | AVDD | P | Analog Supply, 1.8 V |
| 51,52 | VIN+A,VIN−A | AI | Differential Analog Input Pin for Channel A |
| 55 | VREF | AIO | Voltage Reference Input/Output. |
| 56 | SENSE | AI | Reference Mode Select. |
| 57 | VCM | AO | Chip Output. Common mode voltage used to provide analog input |
| 58 | RBIAS | AI | Analog Current Bias. Grounded with a 10 kΩ (1%) resistor |
| 61,62 | VIN−B,VIN+B | AI | Differential Analog Input Pin for Channel B. |

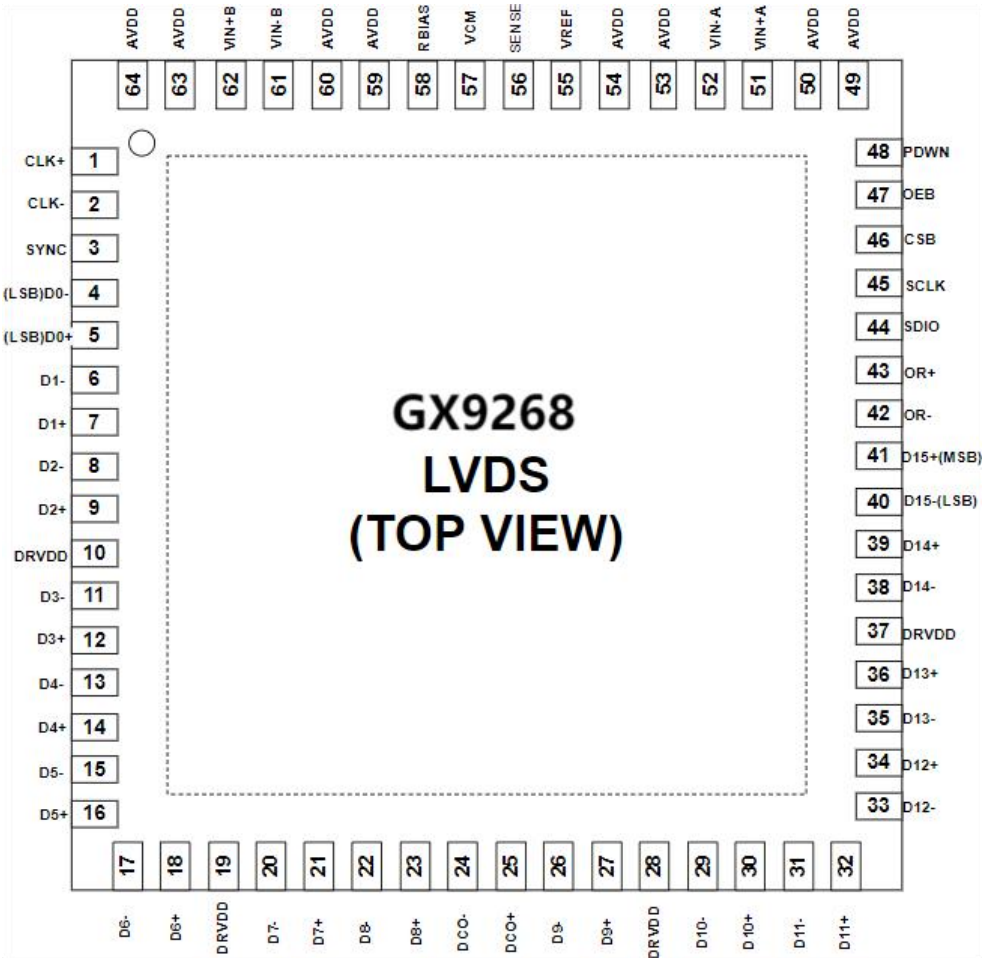



Figure 7 LVDS Pin Configuration

Table 7 LVDS Pin Function Description

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 0 | GND | G | Analog Ground. The pad on the bottom of the package provides the analog ground for the part. This bottom pad must be connected to ground for proper operation. |
| 1,2 | CLK−, CLK+ | AI | Differential Clock Input |
| 3 | SYNC | DI | Digital Input. Synchronous input clock divider |
| 4,5,6,7 | NC | - | Float |
| 4 to 9, 11 to 18, 20 to 23, 26, 27, 29 to 36, 38 to 41 | D0-/+ to D15+/- | DO | LVDS Output Data |
| 10, 19, 28, 37 | DRVDD | P | Digital Output Driver Supply. 1.8V Nominal |
| 42,43 | OR-/+ | DO | LVDS Overrange Data Output |
| 24,25 | DCO-/+ | DO | LVDS Data Clock Output |
| 44 | SDIO | DIO | SPI Data I/O |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 45 | SCLK | DI | SPI Clock Input |
| 46 | CSB | DI | SPI Chip Select. Active low, 30 kΩ internal pull-up |
| 47 | OEB | DO | Digital Input. If logic low, Channel A and Channel B output Data; if logic high, three-state output. 30kΩinternal pull-down. |
| 33 | PDWN | DI | Digital Input. 30kΩinternal pull-down. |
| | | | PDWN high = power-down |
| | | | PDWN low = operation |
| 49, 50, 53, 54, 59, 60, 63, 64 | AVDD | P | Analog Supply, 1.8 V |
| 51,52 | VIN+A,VIN−A | AI | Analog Input Pin for Channel A. |
| 55 | VREF | AIO | Voltage Reference Input/Output. |
| 56 | SENSE | AI | Reference Mode Select. |
| 57 | VCM | AO | Analog input common mode |
| 58 | RBIAS | AI | Analog Current Bias. Grounded with a 10 kΩ (1%) resistor |
| 61,62 | VIN−B,VIN+B | AI | Analog Input Pin for Channel B. |

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD=1.8 V、DRVDD=1.8 V、VIN=−1.0 dBFS differential input, 1.0 V internal reference,

$T_A$=27ºC ,unless otherwise noted.

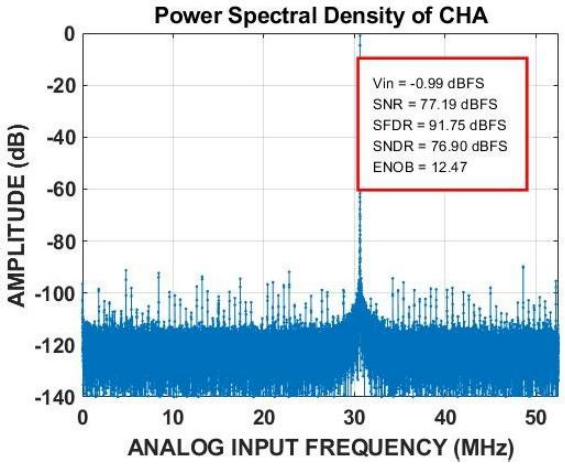



Figure 10 Single-Tone FFT (fin = 30.5MHz@105MSPS)

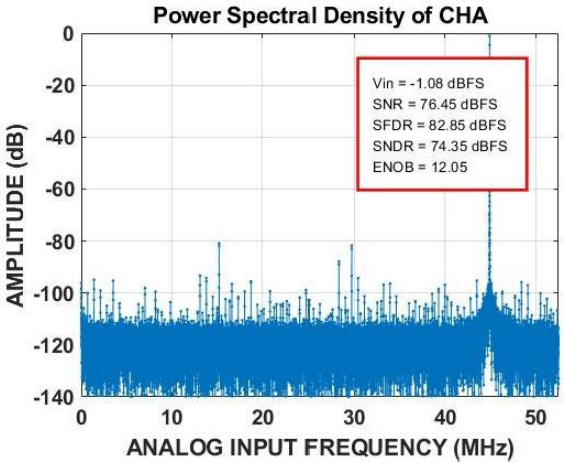



Figure 11 Single-Tone FFT (fin = 60MHz@105MSPS)

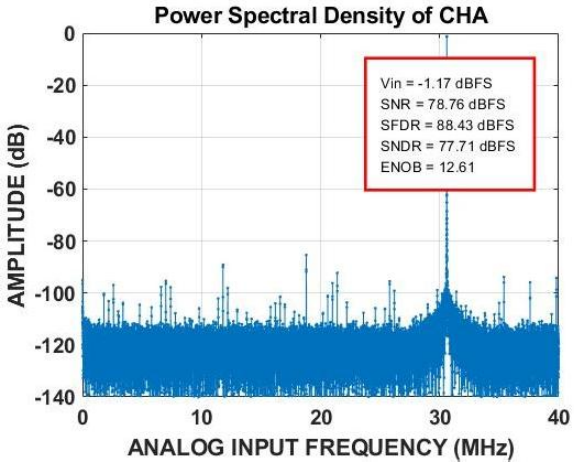



Figure 12 Single-Tone FFT (fin = 30.5MHz@80MSPS)

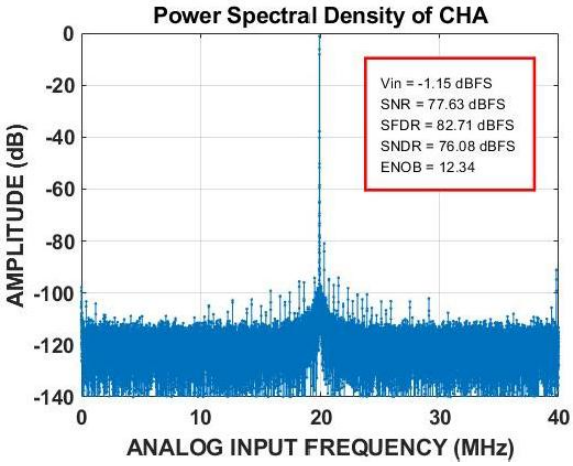



Figure 13 Single-Tone FFT(fin = 60MHz@80MSPS)

# TYPICAL APPLICATION CIRCUITS

The typical application circuits of GX9268 such as input signals, input clocks, external DC pins and peripheral devices are as follows.

**Analog Input Considerations**

Using fully differential mode can ensure optimal ADC performance. To bias the analog input, the VCM voltage can be connected to the center tap of the transformer secondary winding. For applications greater than 10MHz, the coupled differential Dual Balun input is recommended as shown in figure 12. Full differential operational amplifiers can also be used to drive ADC.

In single port applications, using the input network method of VIN- connected to common mode voltage and VIN+ connected to input signal may result in a decrease in ADC performance. Therefore, it is not recommended to drive the GX9268 input at a single port.

In any configuration, the value of parallel capacitor C depends on the input frequency and source impedance, and may need to be reduced or removed. Table 8 shows the recommended values for setting up RC networks. However, these values depend on the input signal and are recommended as application guidelines only.

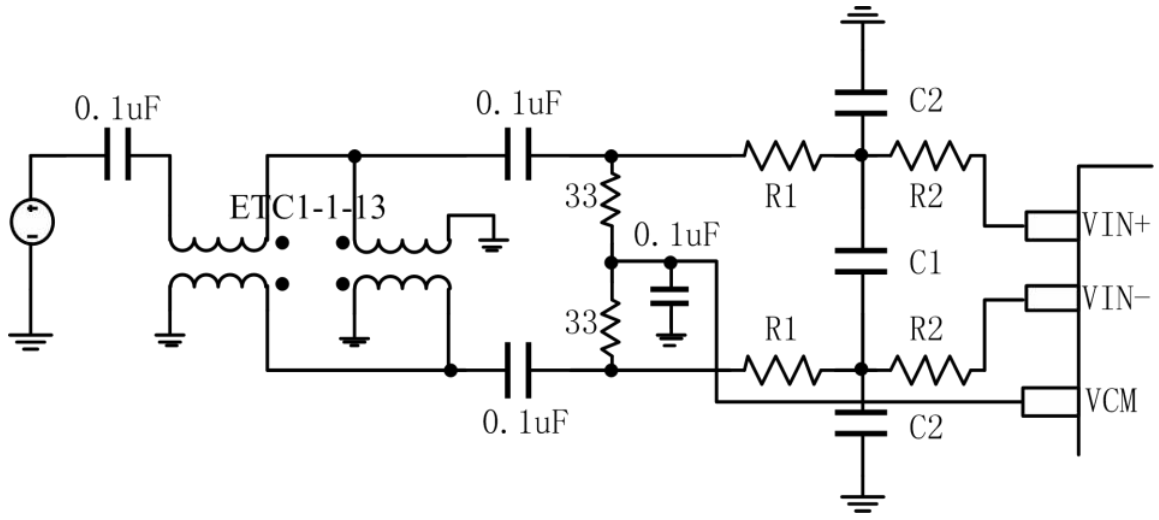



Figure12 Dual Balun-Coupled Input Configuration

Table 8 RC Example Network

| Sampling Frequency (MSPS) | Series Resistor R1/Ω | Series Resistor R2/Ω | Differential Capacitor C1/pF | Shunt Capacitor C2/pF |
|---|---|---|---|---|
| 0-80 | 33 | 15 | 5 | 15 |
| 80-125 | 10 | 15 | 5 | 10 |

### Clock Input Considerations

For optimum performance, the GX9268 sample clock inputs, CLK+ and CLK−, should be clocked with a differential signal. Clock input circuits are biased internally and require no external bias. The balun driver input is recommended as shown in figure 13. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the GX9268 to approximately 0.8 $V_{pp}$ differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the GX9268 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

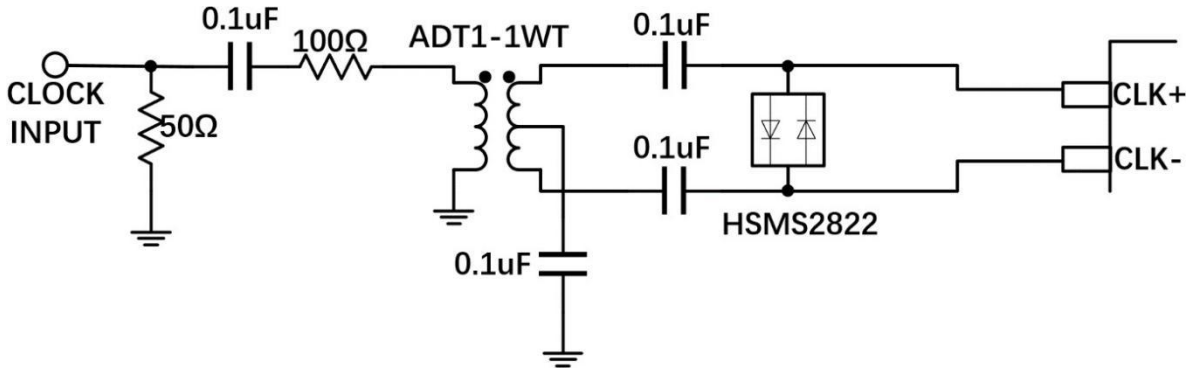



Figure 13 Clock Input Configuration

### Reference Configuration

A comparator within the GX9268 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the internal reference is selected, and the value is 1V; If SENSE connects with AVDD, the external reference is selected, and the value is 1V. It is recommended not to let the SENCE pin float.

Table 9 Reference Configuration Summary

| Selected Mode | SENSE Voltage | Resulting VREF（V） | Resulting Differential Span（Vpp） |
|---|---|---|---|
| External Reference | AVDD | 1.0（Applied to external VREF pin） | 2.0 |
| Internal Reference | AGND to 0.2 | 1.0（Applied to internal VREF pin） | 2.0 |

**Digital Outputs**

The GX9268 output drivers can be configured to interface with 1.8 V CMOS logic families and can also be configured for LVDS outputs. CMOS output data can also be multiplexed onto a single output bus to reduce the total number of channels required to connect the digital processing end, The timing is shown in Figures 2 and 3. The output driver should be able to provide sufficient output current to drive various logic circuits, and the driving force can be adjusted through registers. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

Table 10 Output Data Format

| Input（V） | Condition | Offset Binary Output Mode | Twos complement Mode | OR |
|---|---|---|---|---|
| VIN+ - VIN- | < -VREF – 0.5LSB | 00 0000 0000 0000 | 10 0000 0000 0000 | 1 |
| VIN+ - VIN- | = -VREF | 00 0000 0000 0000 | 10 0000 0000 0000 | 0 |
| VIN+ - VIN- | =0 | 10 0000 0000 0000 | 00 0000 0000 0000 | 0 |
| VIN+ - VIN- | =+VREF – 1LSB | 11 1111 1111 1111 | 01 1111 1111 1111 | 0 |
| VIN+ - VIN- | > +VREF – 0.5LSB | 11 1111 1111 1111 | 01 1111 1111 1111 | 1 |

**Digital Output Enable Function (OEB)**

The GX9268 has a flexible 3-state ability for the digital output pins. The three-state mode is enabled using the OEB pin or through the SPI. If the OEB pin is low, the output IO and DCO are enabled. If the OEB pin is high, the output IO and DCO are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage. When using the SPI, the data outputs and DCO of each channel can be independently three-stated by using the output enable bar bit (Bit 4) in Register 0x14.

**Timing**

The GX9268 provides latched data with a pipeline delay of 19 clock cycles. Data outputs are available one propagation delay ($t_{PD}$) after the rising edge of the clock signal. The length of the output data lines and loads placed on them should be minimized to reduce transients within the GX9268. These transients can degrade converter dynamic performance. The lowest typical conversion rate of the GX9268 is 3 MSPS. At clock rates below 3 MSPS, dynamic performance can degrade.

**Data Clock Output（DCO）**

The GX9268 provides two data clock output (DCO) signals intended for capturing the data in an external register. In CMOS output mode, the data outputs are valid on the rising edge of DCO, unless the DCO clock

polarity has been changed via the SPI. See Figure 2 and Figure 3 for a graphical timing description of the output modes.

**Built-in Self-test (BIST)**

The BIST is a thorough test of the digital portion of the selected GX9268 signal path. Perform BIST testing after resetting to ensure that the component is in a known state. When enabled, the test runs from an internal pseudorandom noise (PN) source through the digital datapath starting at the ADC block output. The BIST sequence runs for 512 cycles and stops. Once completed, BIST will compare the signature results with predetermined values. If the signature matches, BIST sets bit 0 of register 0x24 to indicate that the test passed. If the BIST test fails, bit 0 of register 0x24 is cleared.

The outputs are connected during this test, so the PN sequence can be observed as it runs. Write the value 0x05 to register 0x0E to run BIST. This will enable bit 0 of register 0x0E (BIST enabled) and reset the PN sequence generator, bit 2 of register 0x0E (BIST INIT). When BIST is completed, bit 0 of register 0x24 is automatically cleared. By writing 0 in bit 2 of register 0x0E, the PN sequence can be continued from the last value. However, if the PN sequence is not reset, the signature calculation is not equal to the predetermined value at the end of the test. At this point, the user needs to rely on verifying the output data.

**Output Test Modes**

The output test options of address 0x0D are shown in Table 11. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks, and the test pattern is run through the output formatting block.

Some of the test patterns are subject to output formatting, and some are not. The seed value for the PN sequence tests can be forced if the PN reset bits are used to hold the generator in reset mode by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock.

## SERIAL PORT INTERFACE (SPI)

The GX9268 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. Addresses are accessed via the serial port and can be written to or read from via the port. Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin. The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles. The timing requirements are shown in Figure 5.

### Internal Register Table

Table 11 Register Table

| Address (HEX) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value (HEX) | Default Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Port Configuration | 0 | LSB first | Soft Reset | 1 | 1 | Soft Reset | LSB First | 0 | 0x18 | LSB-first mode or MSB-first mode registers |
| 0x01 | Chip ID | chip ID 0x32 | | | | | | | | 0x32 | Chip grade ID used to differentiate devices; read only |
| 0x02 | Chip Grade | | 010 = 105MSPS<br>011=80MSPS | | | | | | | | Speed grade ID used to differentiate devices; read only |
| 0x05 | Channel Index | | | | | | | Data Channel B | Data Channel A | 0x03 | Bits are set to determine which device on the chip receives the next write command ; The default value is all |

| Address (HEX) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value (HEX) | Default Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | channels on the chip |
| 0x08 | Mode | External Power-down enable | External pin function 0x00full power-down 0x01 standby | | | | | 00 = chip run 01 = full power-down 10 = standby 11 = digital reset | | 0x80 | Determine various generic modes of chip operation |
| 0x0B | Clock Divide | | | | | | Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 1 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 5 110 = divide by 6 111 = divide by 7 | | | 0x00 | |
| 0x0D | Test Mode | User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once | | Reset PN long sequence | Reset PN short sequence | Output test mode:0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1x sync 1011 = one bit high 1100 = mixed bit frequency | | | | 0x00 | When this register is set, the test data is placed on the output pins in place of normal data. |
| 0x0E | BIST Enable | | | | | | BIST INIT | | BIST enable | 0x00 | Whether to activate BIST function |
| 0x0F | ADC_INPUT | | | | | | | | Common mode | 0x00 | |

| Address (HEX) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value (HEX) | Default Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | servo enable | | |
| 0x10 | Offset Adjust | 8-bit device offset adjustment [7:0]<br>Offset adjust in LSBs from +127 to −128 (twos complement format) | | | | | | | | 0x00 | Offset adjust |
| 0x14 | ADC Output Mode | Drive strength<br>0 = ANSI LVDS;<br>1 = reduced swing LVDS | Output type<br>0 = CMOS<br>1 = LVDS | CMOS output Interleaved enable | Output disable | | Output Invert | 00 = offset binary<br>01 = twos complement<br>10 = gray code<br>11 = offset binary | | 0x00 | Configure the outputs and the format of the data |
| 0x16 | Phase Control | DCO output polarity<br>0 = normal<br>1 = inverted | | | | | Input clock phase adjust [2:0] (Value is number of input clock cycles of phase delay)<br>000 = no delay<br>001 = 1 input clock cycle<br>010 = 2 input clock cycles<br>011 = 3 input clock cycles<br>100 = 4 input clock cycles<br>101 = 5 input clock cycles<br>110 = 6 input clock cycles<br>111 = 7 input clock cycles | | | 0x00 | Determine which phase of the divider be used as clock output when used on global clock division device. Internal locking not affected |
| 0x17 | Output Delay | | DATA_Delay<br>000 = 0.29 ns<br>001 = 0.58 ns<br>010 = 0.87 ns<br>011 = 1.16 ns<br>100 = 1.45 ns<br>101 = 1.74 ns<br>110 = 2.03 ns<br>111 = 2.32 ns | | | | DCO_Delay<br>000 = 0.29 ns<br>001 = 0.58 ns<br>010 = 0.87 ns<br>011 = 1.16 ns<br>100 = 1.45 ns<br>101 = 1.74 ns<br>110 = 2.03 ns<br>111 = 2.32 ns | | | 0x00 | Set the fine output delay of the output clock, but it will not change the internal Partial timing |

| Address (HEX) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value (HEX) | Default Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x19 | USER_PATT1_LSB | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User Defined Mode，1 LSB |
| 0x1A | USER_PATT1_MSB | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User Defined Mode，1 MSB |
| 0x1B | USER_PATT2_LSB | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User Defined Mode，2 LSB |
| 0x1C | USER_PATT2_MSB | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User Defined Mode，2 MSB |
| 0x24 | MISR_LSB | | | | | | | | B0 | 0x00 | Least significant byte of MISR；Read only. |
| 0x2A | Feature | | | | | | | | OR Output Enable | 0x01 | Disable index channel OR pin. |
| 0x2E | Output Control | | | | | | | | 0 = ADC A 1 = ADC B | Ch A = 0x00 Ch B = 0x01 | Assign ADC to output channel. |
| 0x100 | Sync Control | | | | | | Clock divider next sync only | Clock divider sync enable | Master sync enable | 0x01 | |
| 0x101 | USR2 | Enable OEB Pin 47 | | | | | | | | 0x80 | |

# APPLICATIONS INFORMATION

### Power And Gound Recommendations

When connecting power to the GX9268, it is recommended that two separate supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length. A single PCB ground plane should be sufficient when using the GX9268. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved

### Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB should mate to the GX9268 exposed paddle. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged to prevent solder wicking through the vias, which can compromise the connection. To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB.

### VCM

The VCM pin should be decoupled to ground with a 0.1 μF capacitor.

### RBIAS

The GX9268 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

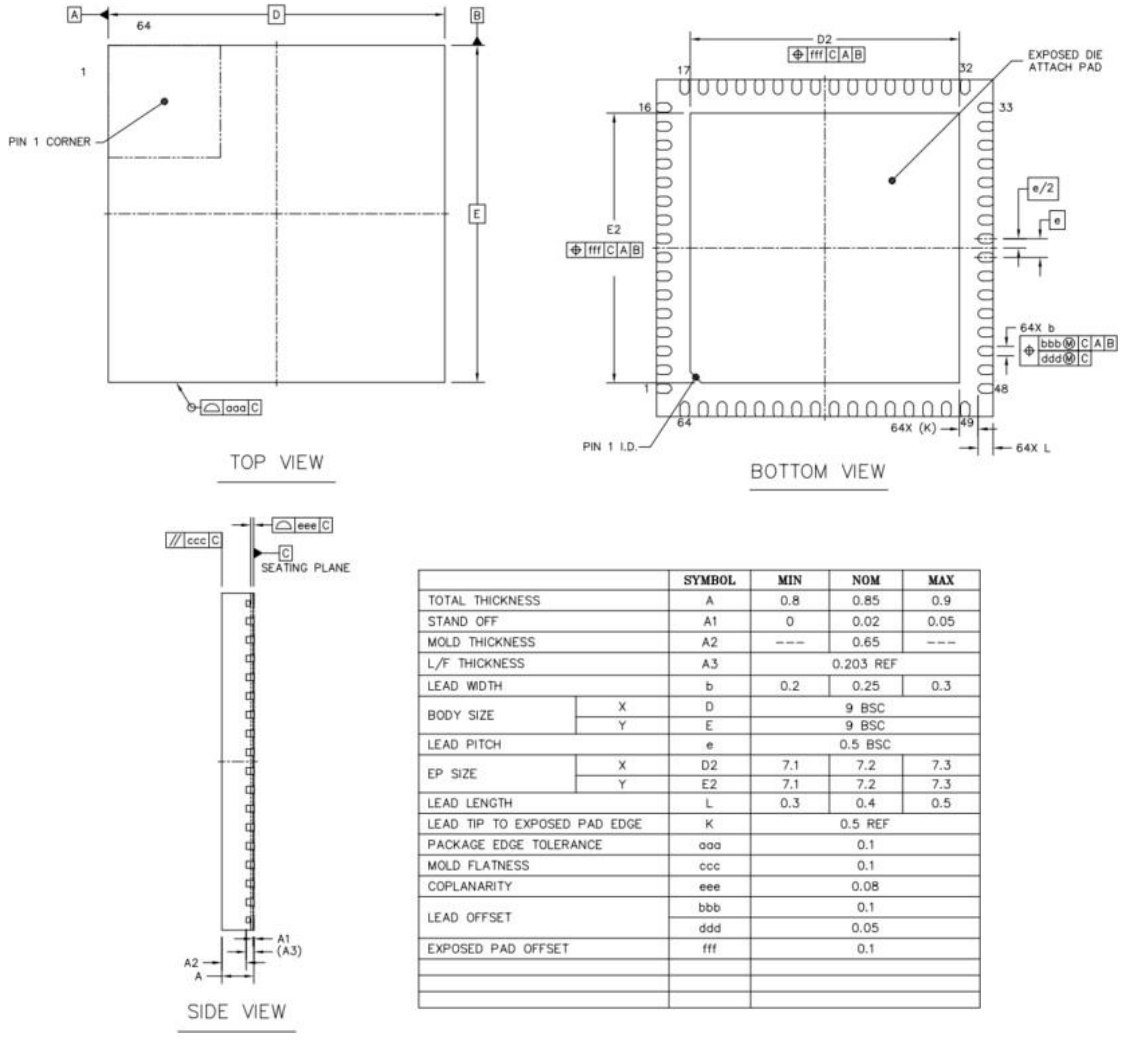
### Reference Decoupling

The VREF pin should be externally decoupled to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

### SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the GX9268 to keep these signals from transitioning at the converter inputs during critical sampling periods.

## OUTLINE DIMENTIONS




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | | 9 BSC | |
| | Y | E | | 9 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | D2 | 7.1 | 7.2 | 7.3 |
| | Y | E2 | 7.1 | 7.2 | 7.3 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.5 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

Figure 16 QFN-64 (Dimensions Shown in Millimeters)

## ORDERING GUIDE

| Part No. | OP Temp | Package |
|---|---|---|
| GX9268GDLUMY-80 | -40 ~ 85℃ | QFN-64 |
| GX9268GDLUMY-105 | -40 ~ 85℃ | QFN-64 |

Note: Packaging can be customized according to customer needs.

# DECLARATION

The above information is for reference only, and is intended to assist GXSC (Shenzhen) Technology Co., Ltd's customers in their research and development. GXSC (Shenzhen) Technology Co., Ltd reserves the right to change the above information without prior notice due to technological innovation.

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