GX9747 Dual 16-Bit 250MSPS DAC

FEATURES

- High dynamic range, dual digital-to-analog converters （DAC）
- Low noise and intermodulation distortion
- Support multiple output modes such as NRZ and RZ
- LVCMOS inputs with dual-port or optional interleaved single-port operation
- Differential analog current outputs are programmable from 8.6 mA to 31.7 mA full-scale
- Auxiliary 10-bit current DAC with source/sink capability
- Internal 1.2 V precision reference voltage source
- Operates from 1.8 V and 3.3 V supplies
- 345 mW power dissipation
- Small footprint, RoHS-compliant, 72-lead LFCSP
- Built in self-calibration function

APPLICATIONS

- Wireless infrastructure:

W-CDMA, CDMA2000, TD-SCDMA, WiMAX

- Wideband communications：

LMDS/MMDS 、 Point-to-point instrumentation, Radio frequency (RF) signal generators, Arbitrary waveform generators

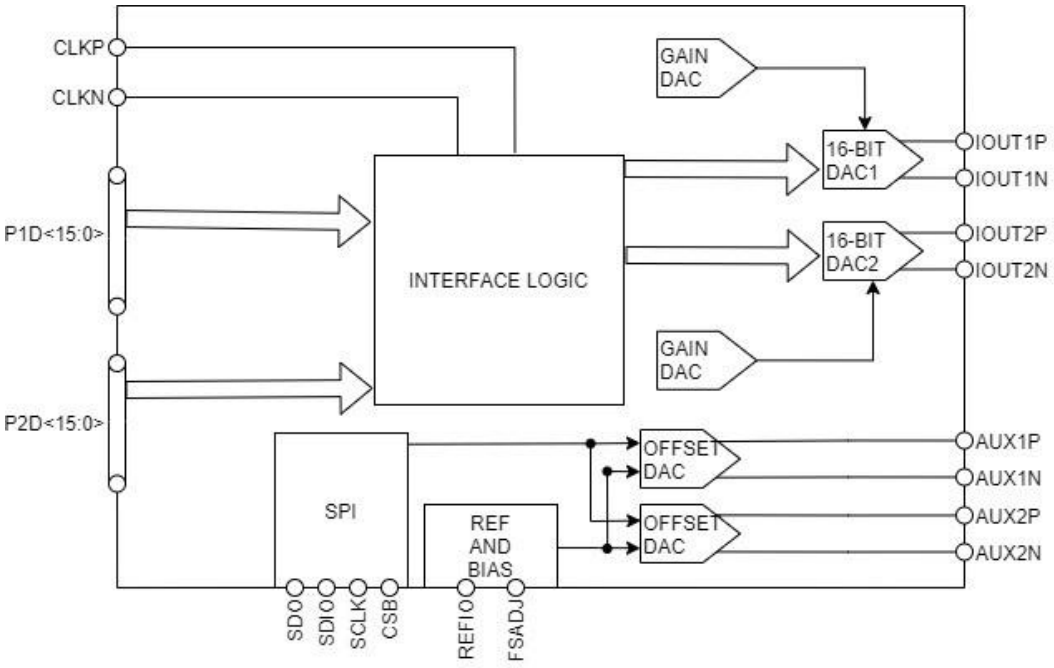

Figure 1 Functional Block Diagram

Version：V1.6
Release Date: 2024/03/07

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GENERAL DESCRIPTION

The GX9747 is high dynamic range, dual DACs with 16-bit resolutions and sample rates of up to 250 MSPS. The devices include specific features for gain and offset compensation, and interface seamlessly with analog quadrature modulators.

A serial peripheral interface (SPI) port provides full programmability. In addition, some pin-programmable features are offered for those applications without a controller. Low noise and intermodulation distortion (IMD) enables high quality synthesis of wideband signals.

Multiple output modes for enhanced dynamic performance.

Programmable current outputs and dual auxiliary DACs provide flexibility and system enhancements.

SPECIFICATIONS

DC Specifications

TMIN to TMAX，AVDD33 = 3.3 V，DVDD33 = 3.3 V，DVDD18 = 1.8 V，CVDD18 = 1.8 V，IFS = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 1 Electric Characteristic-DC Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Resolution			16		Bits
Accuracy					
Differential Nonlinearity (DNL)			±0.5		LSB
Integral Nonlinearity (INL)			±1		LSB
Main DAC Outputs					
Offset Error			±0.001		%FSR
Offset Error Temperature Coefficient			0.1		ppm/℃
Gain Error			±2.0		%FSR
Gain Matching (DAC1 to DAC2)			±1.0		%FSR
Full-Scale Output Current		8.6		31.7	mA
Output Compliance Voltage		-1		1	V
Output Resistance			10		MΩ
Auxiliary DAC Outputs					
Resolution			10		Bits
Full-Scale Output Current		-2		2	mA
Output Compliance Voltage Range—Sink Current		0.8		1.6	V
Output Compliance Voltage Range—Source Current		0		1.6	V
Output Resistance			1.4		MΩ
Monotonicity			10		Bits
Reference Input/Output					
Output Voltage			1.2		V
Output Voltage Temperature Coefficient			10		ppm/℃
External Input Voltage Range		1.15		1.3	V
Input or Output Resistance			5		kΩ
Power Supply Voltage					
AVDD33, DVDD33		3.13		3.47	V
CVDD18, DVDD18		1.7		1.9	V
Power Supply Current					
I_{AVDD33}			69		mA
I_{DVDD33}			4		mA
I_{CVDD18}			16		mA
I_{DVDD18}			41		mA
Power Dissipation					
f_{DAC}=250MSPS, f_{OUT}=20MHz			343		mW
DAC Outputs Disabled			16.5		mW
Full Device Power-Down			1.1		mW
Operating Temperature		-40		125	℃

AC Specifications

TMIN to TMAX，AVDD33 = 3.3 V，DVDD33 = 3.3 V，DVDD18 = 1.8 V，CVDD18 = 1.8 V，IFS = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 2 Electric Characteristic-AC Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Spurious Free Dynamic Range（SFDR）					
f_{DAC}=250MSPS, f_{OUT}=20MHz			79.6		dBc
f_{DAC}=250MSPS, f_{OUT}=70 MHz			70		dBc
f_{DAC}=250MSPS, f_{OUT}=180 MHz			66.8		dBc
Intermodulation Distortion (IMD)					
f_{DAC}=250MSPS, f_{OUT}=20MHz			82		dBc
f_{DAC}=250MSPS, f_{OUT}=70 MHz			79		dBc
f_{DAC}=250MSPS, f_{OUT}=180 MHz			74		dBc

Digital And Timing Specifications

T_{MIN} to T_{MAX}，AVDD33 = 3.3 V，DVDD33 = 3.3 V，DVDD18 = 1.8 V，CVDD18 = 1.8 V，IFS = 20 Ma, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 3 Digital and Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
DAC Clock Inputs (CLKP,CLKN)					
Differential Peak-to-Peak Voltage		400	800	1600	mV
Single-Ended Peak-to-Peak Voltage				800	mV
Common-Mode Voltage		300	400	500	mV
Input Current				1	μA
Input Frequency				250	MHz
Data Clock Output (DCO)					
Output Voltage High		2.4			V
Output Voltage Low				0.4	V
Output Current				10	mA
DAC Clock to Data Clock Output Delay (t_{DCO})		2	2.2	2.8	ns
Data Port Inputs					
Input Voltage High		2.0			V
Input Voltage Low				0.8	V
Input Current				1	uA
Data to DAC Clock Setup Time (t_{DBS} Dual-Port Mode)		400			ps
Data to DAC Clock Hold Time (t_{DBH} Dual-Port Mode)		1200			ps
DAC Clock to Analog Output Data Latency (Dual-Port Mode)				7	Cycles
Data or IQSEL Input to DAC Clock Setup Time (t_{DBS} Single-Port Mode)		400			ps
Data or IQSEL Input to DAC Clock Hold Time (t_{DBH}Single-Port Mode)		1200			ps
DAC Clock to Analog Output Data Latency (Single-Port Mode)				8	Cycles
Serial Peripheral Interface					
SCLK Frequency (f_{SCLK})		10		40	MHz
SCLK Pulse Width High (t_{PWH})		10			ns
SCLK Pulse Width Low (t_{PWL})		1			ns
CSB to SCLK Setup Time (t_S)		0			ns
CSB to SCLK Hold Time (t_H)		1			ns
SDIO to SCLK Setup Time (t_{DS})		0			ns
SDIO to SCLK Hold Time (t_{DH})				1	ns
SCLK to SDIO/SDO Data Valid Time (t_{DV})					ns
RESET Pulse Width Highv		10			ns
Wake-Up Time and Output Latency					
From DAC Outputs Disabled			200		μs
From Full Device Power-Down			1200		μs
DAC Clock to Analog Output Latency (Dual-Port Mode)			7		Cycles
DAC Clock to Analog Output Latency (Single-Port Mode)			8		Cycles

ABSOLUTE MAXIMUM RATINGS

AVDD33, DVDD33 ……..…… -0.3V to 3.6V

DVDD18, CVDD18……..……-0.3V to 1.98V

AVSS,DVSS,CVSS…….....…-0.3V to 0.3V

REFIO…… -0.3V to AVDD33+0.3V

IOUT1P,IOUT1N,IOUT2P,IOUT2N,AUX1P,AUX2N,AUX2P.AUX2N..... -0.1V to AVDD33+0.3V

P1D15 to P1D0, P2D15 to P2D0…….... -0.3V to DVDD33+0.3V

CLKP,CLKN…… ... -0.3V to CVDD18+0.3V

RESET,CSB,SCLK,SDIO,SDO……..…-0.3V to DVDD33+0.3V

Junction Temperature…… ……125°C

Storage Temperature Range……-65°C to 150°C

ATTENTION: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

ESD CAUTION

This product is an electrostatic sensitive device. Therefore, proper ESD precaution measures should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

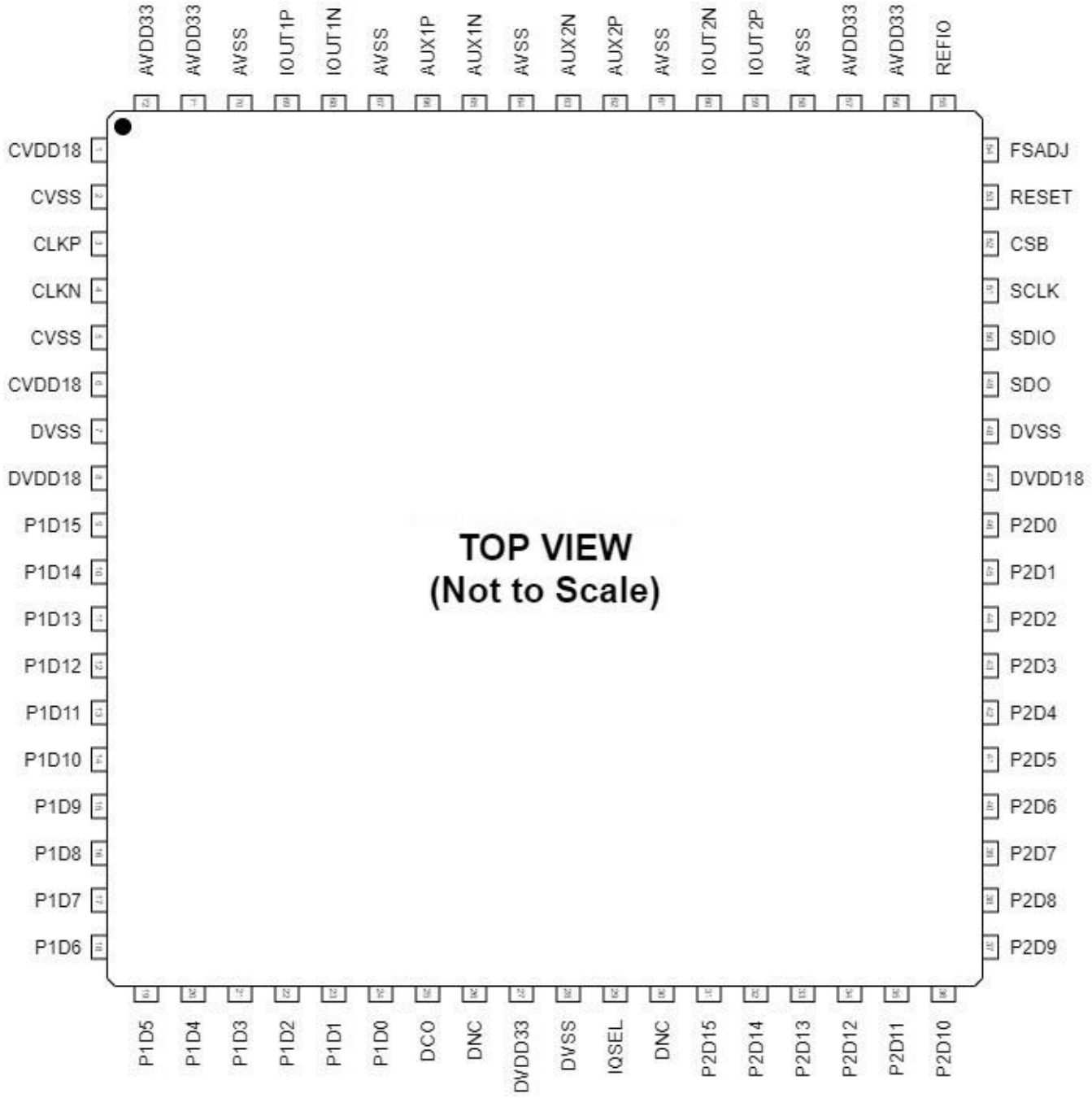


Figure 2 GX9747 Pin Configuration Table 4

Pin Function Description

Pin No.	Mnemonic	Type	Description
1，6	CVDD18	P	Clock Supply Voltage (1.8 V).
2，5	CVSS	G	Clock Supply Common (0 V).
3	CLKP	AI	Differential DAC Clock Input.
4	CLKN	AI	Complementary Differential DAC Clock Input.

Pin No.	Mnemonic	Type	Description
7，28，48	DVSS	G	Digital Supply Common (0 V).
8，47	DVDD18	P	Digital Supply Voltage (1.8 V).
9 to 24	P1D15,PID14,PID13,PID12,PID11,PID10,P1D9,P1D8,P1D7,P1D6,P1D5,P1D4,P1D3,P1D2,P1D1,P1D0	DI	Port 1 Data Bit Inputs.
25	DCO	DO	Data Clock Output. Use to clock data source.
26，30	DNC	/	Do Not Connect.
27	DVDD33	P	Digital Input/Output Supply Voltage (3.3 V).
29	IQSEL	DI	I/Q Framing Signal for Single-Port Mode Operation.
31 to 46	P2D15, P2D14, P2D13, P2D12, P2D11,P2D10,P2D9,P2D8,P2D7,P2D6,P2D5,P2D4,P2D3,P2D2,P2D1,P2D0	DI	Port 2 Data Bit Inputs.
49	SDO	DIO	Serial Peripheral Interface Data Output.
50	SDIO	DI	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	DI	Serial Peripheral Interface Clock Input.
52	CSB	DI	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	DI	Hardware Reset. Active high.
54	FSADJ	AO	Full-Scale Current Output Adjust. Connect a 10 kΩ resistor to AVSS.
55	REFIO	AIO	Reference Input/Output. Connect a 0.1 μF capacitor to AVSS.
56，57，71，72	AVDD33	P	Analog Supply Voltage (3.3 V).
58，61，64，67，70	AVSS	G	Analog Supply Common (0 V).
59	IOUT2P	AO	DAC2 Current Output True. Sources full-scale current when input data bits are all “1”.
60	IOUT2N	AO	DAC2 Current Output Complement. Sources full-scale current when data bits are all “0”.
62	AUX2P	AO	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	AO	Auxiliary DAC2 Optional Output Pin.

Pin No.	Mnemonic	Type	Description
65	AUX1N	AO	Auxiliary DAC1 Optional Output Pin.
66	AUX1P	AO	Auxiliary DAC1 Default Current Output Pin.
68	IOUT1N	AO	Complementary DAC1 Current Output. Sources full-scale current when data bits are all “0”.
69	IOUT1P	AO	DAC1 Current Output. Sources full-scale current when data bits are all “1”.
	EPAD	G	Exposed Thermal Pad. The exposed thermal pad must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

THEORY OF OPERATION

All features and options are software programmable through the SPI port.

SPI Port

The SPI port is a flexible, synchronous serial communications port, single or multiple byte transfers are supported as well as MSB-first or LSB-first transfer formats. Accomplish serial data input/output through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

Instruction Byte

The instruction byte contains the information shown in the following bit map.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
R/W	N1	N0	A4	A3	A2	A1	A0

Bit 7, R/W, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

Bits [6:5], N1 and N0, determine the number of bytes to be transferred during the data transfer cycle. The bits decode as shown in Table 5.

Table 5. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

Bits [4:0], A4, A3, A2, A1, and A0, determine which register is accessed during the data transfer of the communications cycle. For multibyte transfers, this address is a starting or ending address depending on the current data transfer mode.

MSB/LSB Transfers

The serial port can support both MSB-first and LSB-first data formats, as shown in figure 3 and figure 4.

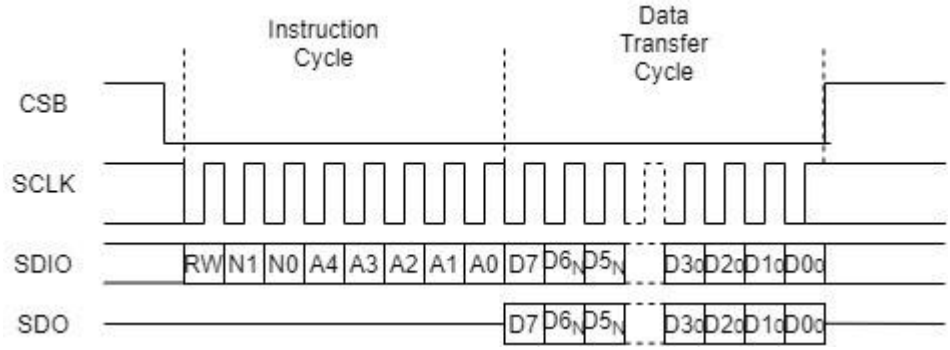


Figure 3 MSB First

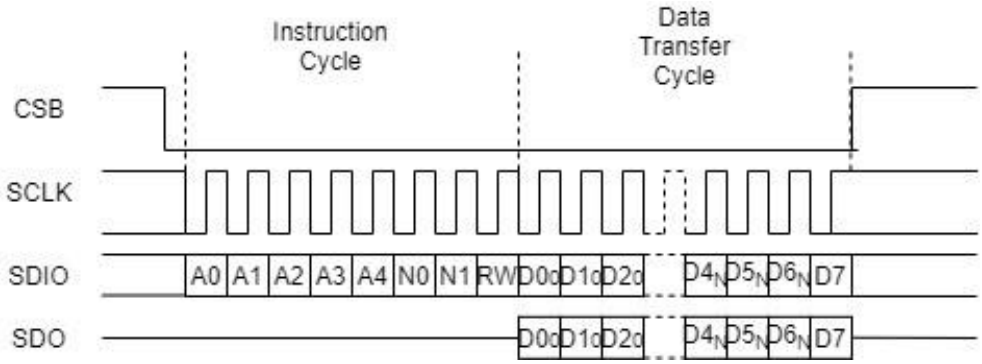


Figure 4 LSB First

Dual-port Mode Timing

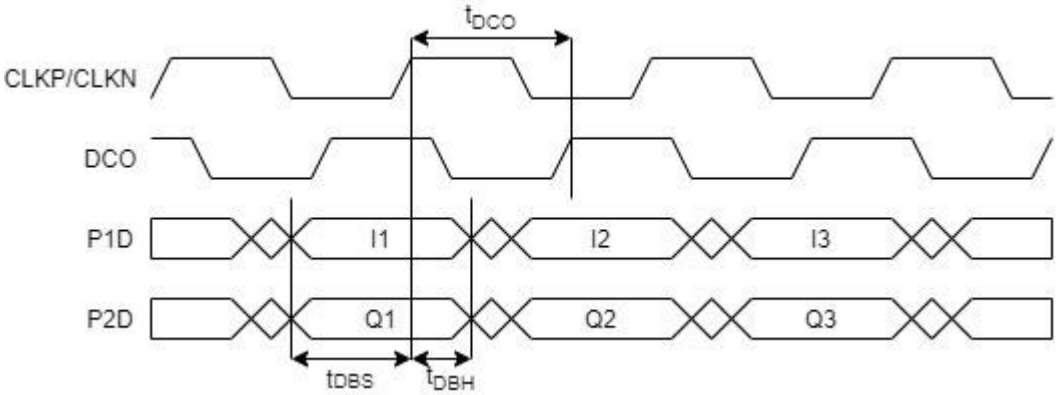


Figure 5 Dual-Port Mode Timing Diagram

In figure 5, Data for DAC1 and DAC2 are input by P1D and P2D respectively.

Single-port Mode Timing

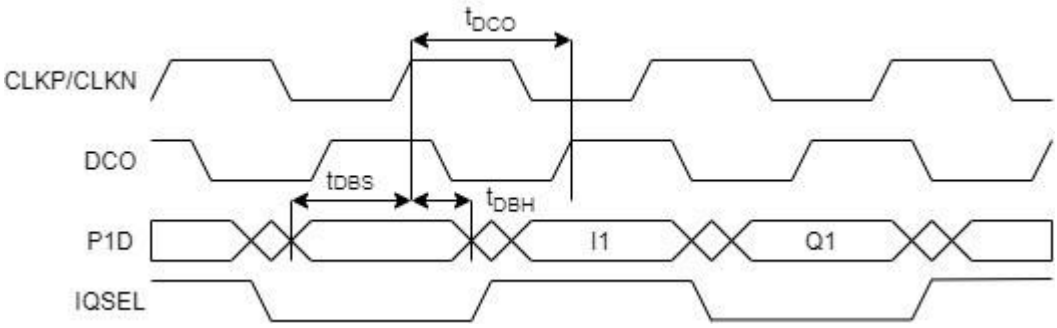


Figure 6 Single-Port Mode Timing Diagram

As shown in figure 6, in single-port mode, data for both DACs is received on the Port 1 input bus. When IQSEL is high, data is steered to DAC1 and when IQSEL is low, data is steered to DAC2. IQSEL must coincide as well as be time-aligned with incoming data

SPI Port, RESE And Pin Mode

Once the RESET pin goes low, the SPI port can activate and, the functions of the device can be configured through SPI.

For applications without a controller, the GX9747 also support pin mode operation, which allows some functional options to be pin, selected without the use of the SPI port. Pin mode is enabled anytime the RESET pin is held high. In pin mode, the four SPI port pins take on secondary functions, as shown in

Table 6.

Table 6 SPI Pin Functions

Pin Name	Description
SCLK	ONEPORT（0x02，Bit6）equals pin state 0：Logic Low 1：Logic High
SDIO	DATTYPE（0x02，Bit7）equals pin state 0：Logic Low 1：Logic High
CSB	Enable mix mode, if CSB is high, Register 0x0A is set to 0x05.
SDO	Enable full power-down, if SDO is high, Register 0x03 is set to 0xFF.

REGISTER

Table 7 Register Table

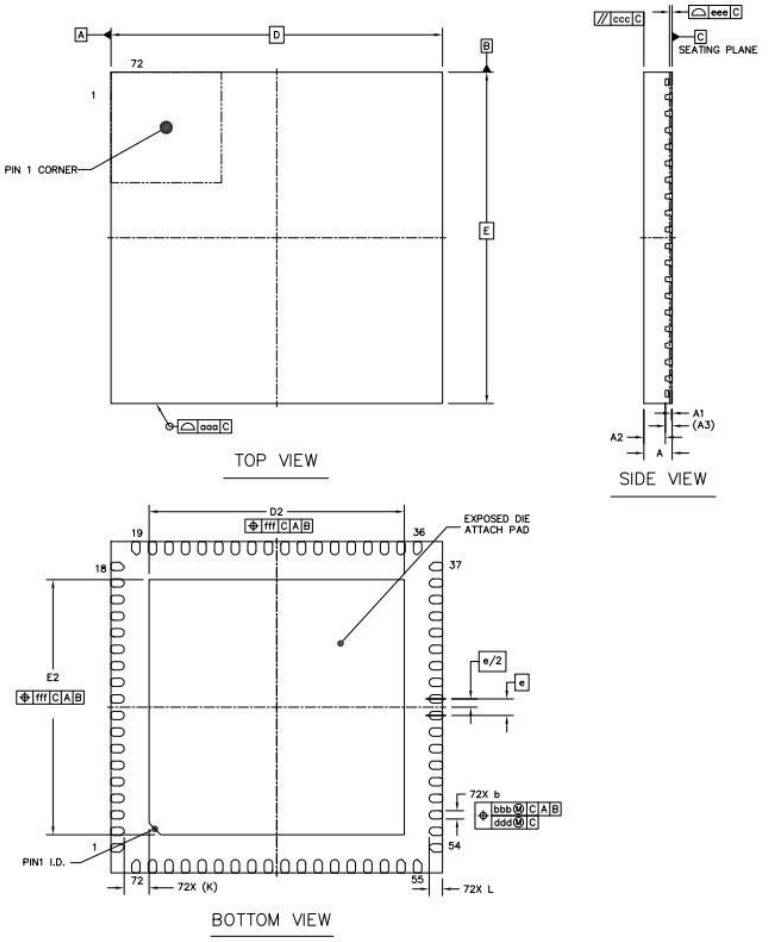
ADDRESS Bits	REGISTER NAME	DEFAULT VALUE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	SPI Control	00h	SDIODIR	LSBFIRST	SWRESET					
02h	Data Control	00h	DATTYPE	ONEPORT		INVDCO				
03h	Power Down	00h	PD_DCO		PD_AUX2	PD_AUX1	PD_BIAS	PC_CLK	PD_DAC2	PD_DAC1
0Ah	DAC Mode Select	00h					DAC1MOD[1:0]		DAC2MOD[1:0]	
0Bh	DAC1 gain LSB	F9h	DAC1FSC[7:0]							
0Ch	DAC1 Gain MSB	01h							DAC1FSC[9:8]	
0Dh	AUX DAC1 LSB	00h	AUXDAC1[7:0]							
0Eh	AUX DAC1 MSB	00h	AUX1PIN		AUX1DIR				AUXDAC1[9:8]	
0Fh	DAC2 Gain LSB	F9h	DAC2FSC[7:0]							
10h	DAC2 Gain MSB	01h							DAC2FSC[9:8]	
11h	AUX DAC2 LSB	00h	AUXDA2[7:0]							
12h	AUX DAC2 MSB	00h	AUX2PIN		AUX2DIR				AUXDA2[9:8]	

Table 8 Register Description

Register	Address	Bit	Name	Description
SPI Control	0x00	7	SDIODIR	0 = operate SPI in 4-wire mode, SDIO pin operates as an input only 1 = operate SPI in 3-wire mode, SDIO pin operates as a bidirectional input/output line
		6	LSBFIRST	0 = LSBFIRST off, SPI serial data mode is MSB to LSB 1 = LSBFIRST on, SPI serial data mode is LSB to MSB
		5	SWRESET	0 = resume normal operation following software RESET 1 = software RESET; loads default values to all registers (except Register 0x00)
Data Control	0x02	7	DATTYPE	0 = DAC input data is twos complement binary format 1 = DAC input data is unsigned binary format
		6	ONEPORT	0 = normal dual-port input mode 1 = optional single port input mode, interleaved data received on Port 1 only
		4	INVDCO	1 = inverts data clock output signal
Power Down	0x03	7	PD_DCO	1 = power down data clock output
		5	PD_AUX2	1 = power down AUX2 DAC
		4	PD_AUX1	1 = power down AUX1 DAC
		3	PD_BIAS	1 = power down reference voltage bias circuit
		2	PD_CLK	1 = power down DAC clock input circuit
		1	PD_DAC2	1 = power down DAC2 analog output
		0	PD_DAC1	1 = power down DAC1 analog output
DAC Mode Select	0x0A	3:2	DAC1MOD[1:0]	00 = selects normal mode, DAC1 01 = selects mix mode, DAC1 10 = selects return to zero mode, DAC1
		1:0	DAC2MOD[1:0]	00 = selects normal mode, DAC2 01 = selects mix mode, DAC2 10 = selects return to zero mode, DAC2
DAC1 Gain	0x0B	7:0	DAC1FSC[7:0]	DAC1 full-scale 10-bit adjustment
	0x0C	1:0	DAC1FSC[9:8]	0x03FF = sets full-scale current to the maximum value of 31.66 mA 0x01F9 = sets full-scale current to the nominal value of 20.0 mA 0x0000 = sets full-scale current to the minimum value of 8.64 mA
AUX DAC1	0x0D	7:0	AUXDAC1[7:0]	Auxiliary DAC1 10-bit output current adjustment
	0x0E	1:0	AUXDAC1[9:8]	0x03FF = sets output current magnitude to 2.0 mA 0x0200 = sets output current magnitude to 1.0 mA 0x0000 = sets output current magnitude to 0.0 mA

Register	Address	Bit	Name	Description
		7	AUX1PIN	1 = AUX1P output pin is active 0 = AUX1N output pin is active
		6	AUX1DIR	0 = configures AUX1 DAC output to source current 1 = configures AUX1 DAC output to sink current
DAC2 Gain	0x0F	7:0	DAC2FSC[7:0]	DAC2 full-scale 10-bit adjustment
	0x10	1:0	DAC2FSC[9:8]	0x03FF = sets full-scale current to the maximum value of 31.66 mA 0x01F9 = sets full-scale current to the nominal value of 20.0 mA 0x0000 = sets full-scale current to the minimum value of 8.64 mA
AUX DAC2	0x11	7:0	AUXDAC2[7:0]	Auxiliary DAC2 10-bit output current adjustment
	0x12	1:0	AUXDAC2[9:8]	0x03FF = sets output current to 2.0 mA 0x0200 = sets output current to 1.0 mA 0x0000 = sets output current to 0.0 mA
		7	AUX2PIN	1 = AUX2P output pin is active 0 = AUX2N output pin is active
		6	AUX2DIR	0 = configures AUX2 DAC output to source current 1 = configures AUX2 DAC output to sink current

OUTLINE DIMENTIONS



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	7.6	7.7	7.8
	Y	E2	7.6	7.7	7.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.75 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Figure 7 QFN-72 10mmx10mm

ORDERING GUIDE

Table 7 Order Information

Part No.	OP Temp	Package	Packing
GX9747GDLUBY	-40~85℃	QFN-72	Tape & Reel

Note: Packaging can be customized according to customer needs.

DECLARATION

The above information is for reference only, and is intended to assist GXSC (Shenzhen) Technology Co., Ltd customers in their research and development. GXSC (Shenzhen) Technology Co., Ltd reserves the right to change the above information without prior notice due to technological innovation.

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