GX9783 Dual 16-Bit 400MSPS DAC

FEATURES

- High dynamic range, dual digital-to-analog converters （DAC）
- Low noise and intermodulation distortion
- Support multiple output modes such as NRZ and RZ
- LVDS inputs
- Differential analog current outputs are programmable from 8.6 mA to 31.7 mA full-scale
- Auxiliary 10-bit current DAC with source/sink capability
- Internal 1.2 V precision reference voltage source
- Operates from 1.8 V and 3.3 V supplies
- 345 mW power dissipation
- Small footprint, RoHS-compliant, 72-lead LFCSP
- Built in self-calibration function

APPLICATIONS

- Wireless infrastructure:

W-C DMA, CDMA2000, TD-SCDMA, WiMAX

- Wideband communications：LMDS/MMDS
- Point-to-point instrumentation
- Radio frequency (RF) signal generators
- Arbitrary waveform generators

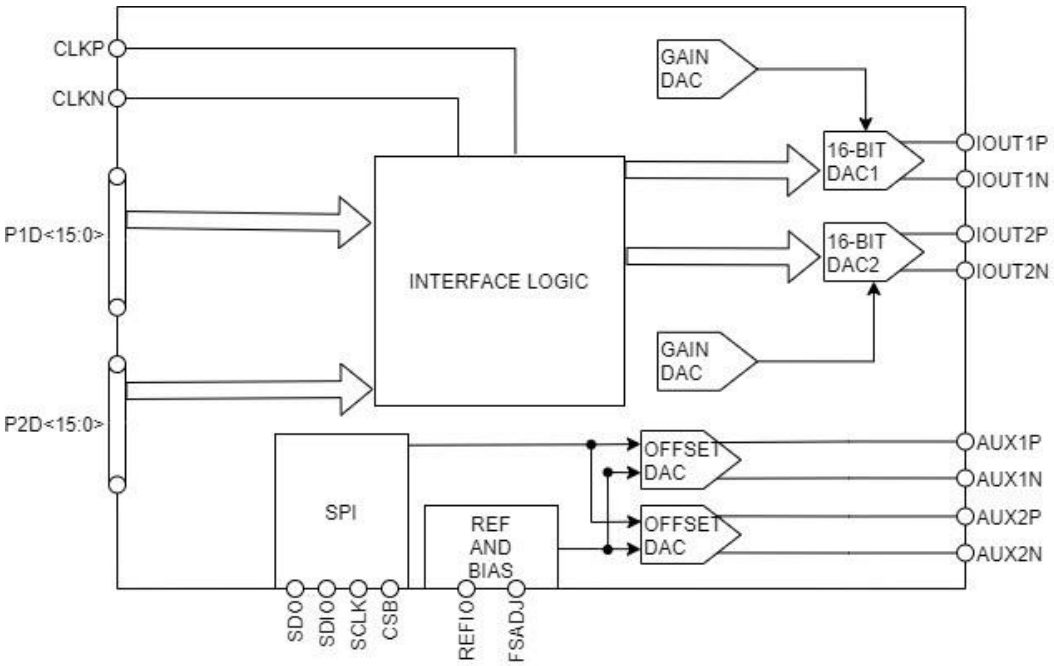

Figure 1 Functional Block Diagram

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GENERAL DESCRIPTION

The GX9783 is high dynamic range, dual DACs with sample rates of up to 400 MSPS. The devices include specific features for gain and offset compensation, and interface seamlessly with analog quadrature modulators.

The GX9783 provides serial peripheral interface (SPI) port. In addition, some pin-programmable features are offered for those applications without a controller. Low noise and intermodulation distortion (IMD) enables high quality synthesis of wideband signals.

Multiple output modes for enhanced dynamic performance.

Programmable current outputs and dual auxiliary DACs provide flexibility and system enhancements.

SPECIFICATIONS

DC Specifications

T_{MIN} to T_{MAX}，AVDD33 = 3.3 V，DVDD33 = 3.3 V，DVDD18 = 1.8 V，CVDD18 = 1.8 V，I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1 Electric Characteristic-DC Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Resolution			16		Bits
Accuracy					
Differential Nonlinearity (DNL)			±0.5		LSB
Integral Nonlinearity (INL)			±1		LSB
Main DAC Outputs					
Offset Error		-0.001	0	+0.001	%FSR
Gain Error (internal reference)			±2.0		%FSR
Full-Scale Output Current		8.66	20.2	31.66	mA
Output Compliance Voltage		-1		1	V
Output Resistance			10		MΩ
Main DAC Monotonicity Guaranteed					
Main DAC Temperature Drift					
Offset		0.04	0.04	0.04	ppm/°C
Gain		100	100	100	ppm/°C
Reference Voltage		30	30	30	ppm/°C
Auxiliary DAC Outputs					
Resolution			10		Bits
Full-Scale Output Current		-2		2	mA
Output Compliance Voltage Range—Sink Current		0		1.6	V
Output Compliance Voltage Range—Source Current		0.8		1.6	V
Output Resistance				1	MΩ
AUX DAC Monotonicity Guaranteed					
Reference					
External Input Voltage Range			1.2		V
Output Resistance			5		kΩ
Analog Supply Voltages					
AVDD33		3.13	3.3	3.47	V
CVDD18		1.70	1.8	1.90	V
Digital Supply Voltage					
DVDD33		3.13	3.3	3.47	V
DVDD18		1.70	1.8	1.90	V
Supply Current					
I_{AVDD33}			55	58	mA
I_{DVDD33}			13	15	mA
I_{CVDD18}			34	38	mA
I_{DVDD18}			68	85	mA
Power Dissipation					
f_{DAC}=400MSPS, IF=20MHz			V*I	V*I	mW
f_{DAC}=400MSPS, IF=10MHz			440		mW
Power-Down Mode			3	35	mW

1. Based on a 10kΩ external resistor.
2. f_{DAC}=400MSPS, f_{OUT}=20MHz

AC Specifications

T_{MIN} to T_{MAX}，AVDD33 = 3.3 V，DVDD33 = 3.3 V，DVDD18 = 1.8 V，CVDD18 = 1.8 V，I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2 Electric Characteristic-AC Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Spurious Free Dynamic Range（SFDR）					
f_{DAC}=400MSPS, f_{OUT}=20MHz			80		dBc
f_{DAC}=400MSPS, f_{OUT}=120 MHz			68		dBc
f_{DAC}=400MSPS, f_{OUT}=380 MHz (Mix Mode)			62		dBc
Two-Tone Intermodulation Distortion (IMD)					
f_{DAC}=400MSPS, f_{OUT}=20MHz			86		dBc
f_{DAC}=400MSPS, f_{OUT}=120 MHz			79		dBc
f_{DAC}=400MSPS, f_{OUT}=380 MHz (Mix Mode)			64		dBc
One-Tone Noise Spectral Density (NSD)					
f_{DAC}=400MSPS, f_{OUT}=40MHz			-165		dBc
f_{DAC}=400MSPS, f_{OUT}=120 MHz			-157		dBc
f_{DAC}=400MSPS, f_{OUT}=380 MHz (Mix Mode)			-154		dBc

Digital And Timing Specifications

T_{MIN} to T_{MAX}，AVDD33 = 3.3 V，DVDD33 = 3.3 V，DVDD18 = 1.8 V，CVDD18 = 1.8 V，IFS = 20 Ma, maximum sample rate, unless otherwise noted.

Table 3 Digital and Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
DAC Clock Input (CLKP, CLKN)					
Differential Peak-to-Peak Voltage		400	800	1600	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate		400			MSPS
DAC Clock to Analog Output Data Latency				7	Cycles
Serial Peripheral Interface (CMOS Interface)					
Maximum Clock Rate (SCLK)				40	MHz
Minimum Pulse Width High				12.5	ns
Minimum Pulse Width Low				12.5	ns
Setup Time, SDI to SCLK (t_{DS})		2.0			ns
Hold Time, SDI to to SCLK (t_{DH})		0.2			ns
Data Valid, SDO to SCLK, (t_{DV})		2.3			ns
Setup time, CSB to SCLK (t_{DCSB})			1.4		ns
Serial Peripheral Interface Logic Levels					
Input Logic High		2.0			V
Input Logic Low				0.8	V
Digital Input Data (LVDS Interface)					
Input Voltage Range, V_{IA} or V_{IB}		800		1600	mV
Input Differential Threshold, V_{IDTH}		-100		+100	mV
Input Differential Hysteresis, V_{IDTHH} to V_{IDTHL}			20		mV

Input Differential Input Impedance, R_{IN}		80	120	Ω
Maximum LVDS Input Rate (per DAC)		400		MSPS

ABSOLUTE MAXIMUM RATINGS

AVDD33, DVDD33 ……..…… -0.3V to 3.6V

DVDD18, CVDD18……..……-0.3V to 1.98V

AVSS,DVSS,CVSS…….....…-0.3V to 0.3V

REFIO…… -0.3V to AVDD33+0.3V

IOUT1P,IOUT1N,IOUT2P,IOUT2N,AUX1P,AUX2N,AUX2P.AUX2N..... -0.1V to AVDD33+0.3V

P1D15 to P1D0, P2D15 to P2D0…….... -0.3V to DVDD33+0.3V

CLKP,CLKN…… ... -0.3V to CVDD18+0.3V

RESET,CSB,SCLK,SDIO,SDO……..…-0.3V to DVDD33+0.3V

Junction Temperature…… ……125°C

Storage Temperature Range……-65°C to 150°C

ATTENTION: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

ESD CAUTION

This product is an electrostatic sensitive device. Therefore, proper ESD precaution measures should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

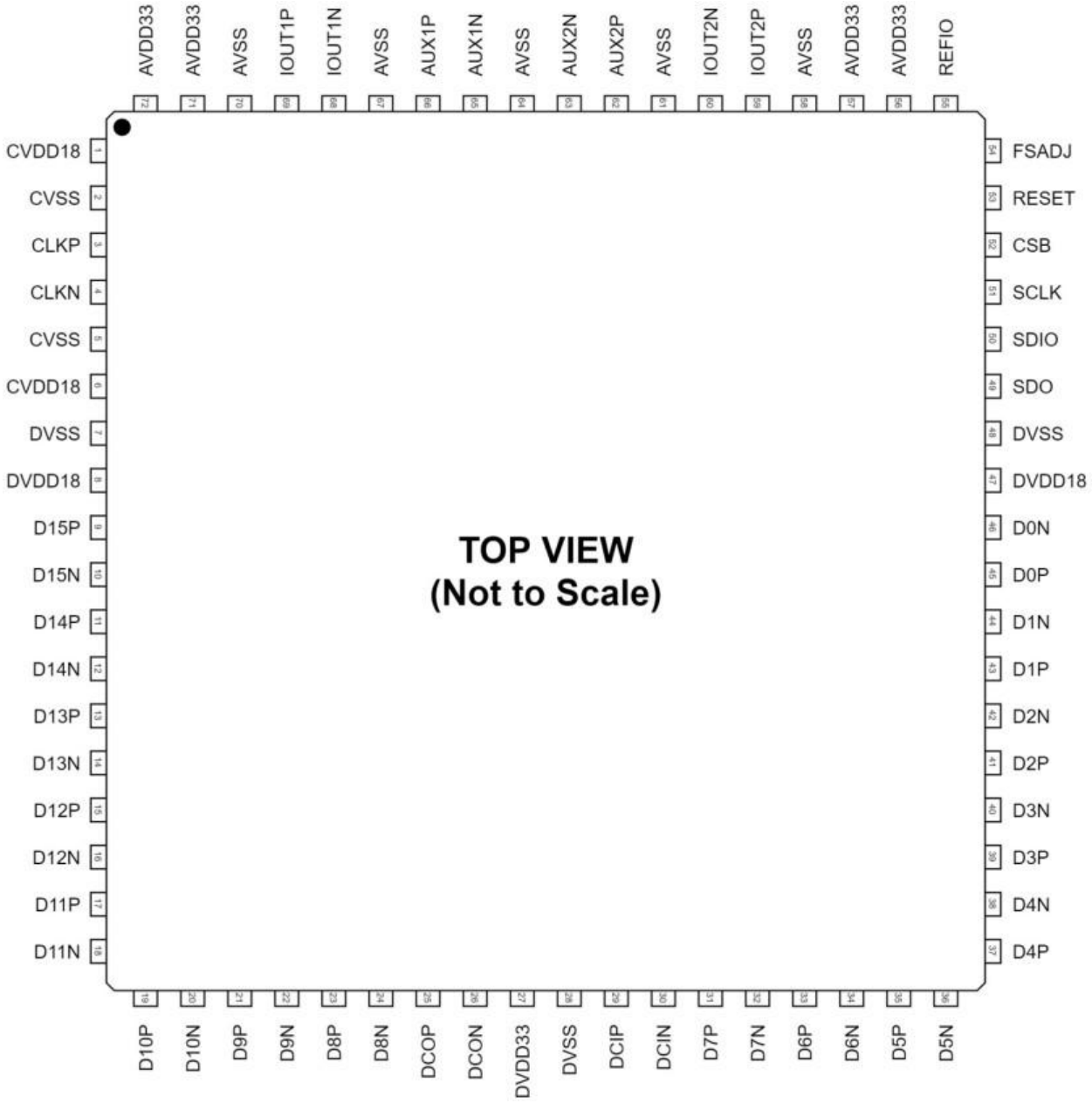


Figure 2 GX9783 Pin

Configuration Table 4 Pin Function

Description

Pin No.	Mnemonic	Type	Description
1, 6	CVDD18	P	Clock Supply Voltage (1.8 V).
2, 5	CVSS	G	Clock Supply Return.
3, 4	CLKP, CLKN	AI	Differential DAC Clock Input.
7, 28, 48	DVSS	G	Digital Supply Common (0 V).

8, 47	DVDD18	P	Digital Supply Voltage (1.8 V).

Pin No.	Mnemonic	Type	Description
9 to 24, 31 to 46	D15P, D15N to D0P, D0N	DI	LVDS Data Inputs. D15 is the MSB, D0 is the LSB.
25, 26	DCOP, DCON	DO	Differential Data Clock Output. Clock at the DAC sample rate.
27	DVDD33	P	Digital Input/Output Supply Voltage (3.3 V).
29, 30	DCIP, DCIN	DI	Differential Data Clock Input. Clock aligned with input data.
49	SDO	DIO	Serial Port Data Output.
50	SDIO	DI	Serial Port Data Input (4-Wire Mode) or Bidirectional Serial Data Line (3-Wire Mode)
51	SCLK	DI	Serial Peripheral Interface Clock Input.
52	CSB	DI	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	DI	Chip Reset. Active high.
54	FSADJ	AO	Full-Scale Current Output Adjust.
55	REFIO	AIO	Analog Reference Input/Output (1.2 V Nominal).
56, 57, 71, 72	AVDD33	P	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	G	Analog Common (0 V).
59	IOUT2P	AO	DAC Current Output. Full-scale current is sourced when all data bits are 1s
60	IOUT2N	AO	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
62, 63	AUX2P, AUX2N	AO	Differential Auxiliary DAC Current Output (Channel 2).
65, 66	AUX1N, AUX1P	AO	Differential Auxiliary DAC Current Output (Channel 1).
68	IOUT1N	AO	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
69	IOUT1P	AO	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
Heat Sink Pad	N/A	G	The heat sink pad on the bottom of the package must be soldered to the PCB plane that carries AVSS.

THEORY OF OPERATION

All features and options are software programmable through the SPI port.

SPI Port

The SPI port is a flexible, synchronous serial communications port, single or multiple byte transfers are supported as well as MSB-first or LSB-first transfer formats. Serial data input/output can be accomplished through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

Instruction Byte

The instruction byte contains the information shown in the following bit map.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
R/W	N1	N0	A4	A3	A2	A1	A0

Bit 7, R/W, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

Bits [6:5], N1 and N0, determine the number of bytes to be transferred during the data transfer cycle. The bits decode as shown in Table 5.

Table 5. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

Bits [4:0], A4, A3, A2, A1, and A0, determine which register is accessed during the data transfer of the communications cycle. For multibyte transfers, this address is a starting or ending address depending on the current data transfer mode.

MSB/LSB Transfers

The serial port can support both MSB-first and LSB-first data formats, as shown in figure 3 and figure 4.

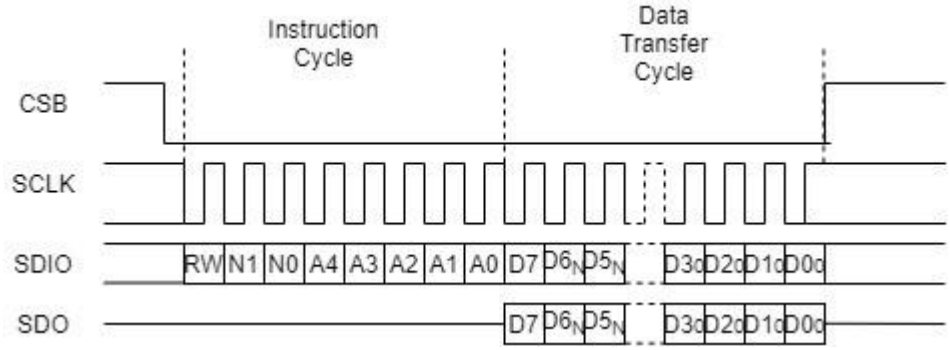


Figure 3 MSB First

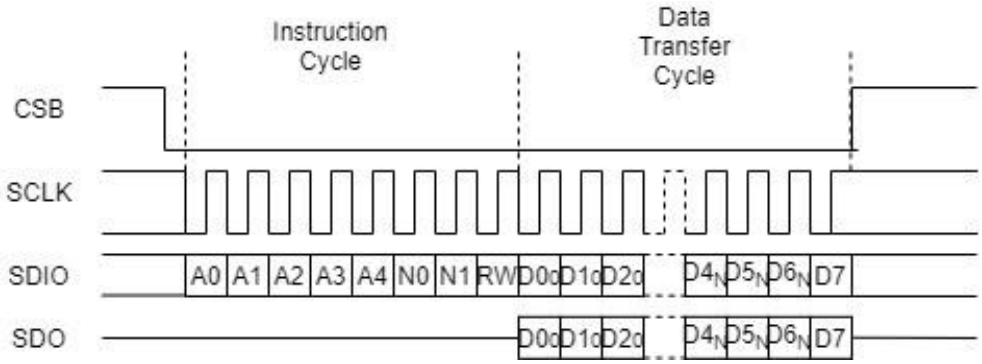


Figure 4 LSB First

Dual-port Mode Timing

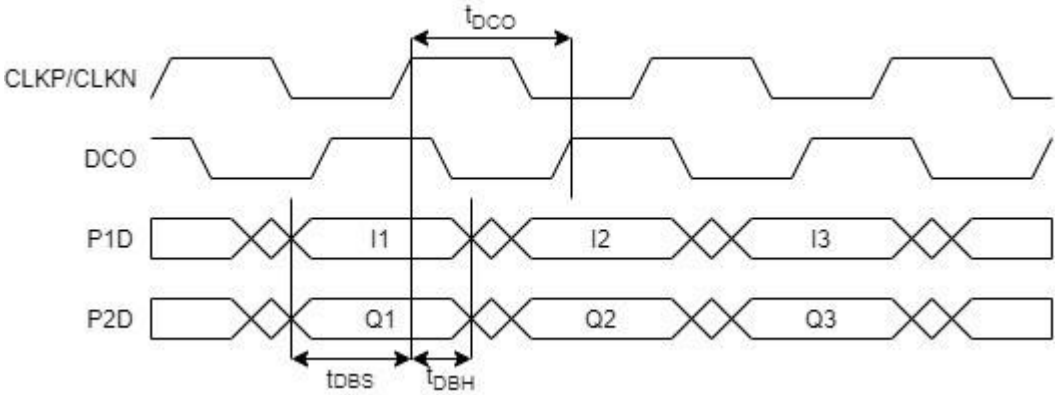


Figure 5 Dual-Port Mode Timing Diagram

In figure 5, Data for DAC1 and DAC2 are input by P1D and P2D respectively.

Single-port Mode Timing

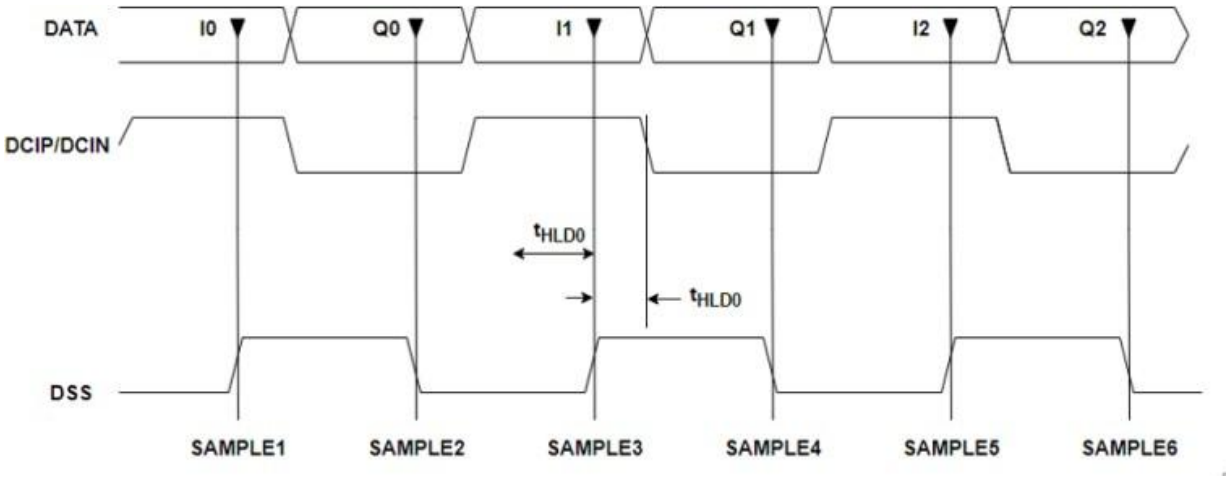


Figure 6 Single-Port Mode Timing Diagram

As shown in figure 6, in single-port mode, data for both DACs is received on the Port 1 input bus. When IQSEL is high, data is steered to DAC1 and when IQSEL is low, data is steered to DAC2. IQSEL must coincide as well as be time-aligned with incoming data

SPI Port, Reset And Pin Mode

Once the RESET pin goes low, the SPI port can be activated, and the functions of the device can be configured through SPI.

For applications without a controller, the SC3361 also support pin mode operation, which allows some functional options to be pin, selected without the use of the SPI port. Pin mode is enabled anytime the RESET pin is held high. In pin mode, the four SPI port pins take on secondary functions, as shown in Table 6.

Table 6 SPI Pin Functions

Pin Name	Description
SCLK	ONEPORT（0x02，Bit6）equals pin state 0：Logic Low 1：Logic High
SDIO	DATTYPE（0x02，Bit7）equals pin state 0：Logic Low 1：Logic High
CSB	Enable mix mode, if CSB is high, Register 0x0A is set to 0x05.

SDO	Enable full power-down, if SDO is high, Register 0x03 is set to 0xFF.

REGISTER

Table 7 Register Table

ADDRESS Bits	REGISTER NAME	DEFAULT VALUE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	SPI Control	00h	SDIODIR	LSBFIRST	RESET					
02h	Data Control	00h	DATA			INVDCO				
03h	Power Down	00h	PD_DCO	PD_INPT	PD_AUX2	PD_AUX1	PD_BIAS	PC_CLK	PD_DAC2	PD_DAC1
04h	Setup and Hold	00h	SET[3:0]				HLD[3:0]			
05h	Timing Adjust	00h				SAMP_DLY[4:0]				
06h	Seek	00h						LVDS low	LVDS high	SEEK
0Ah	Mix Mode	00h					DAC1MIX[1:0]		DAC2MIX[1:0]	
0Bh	DAC1 FSC	F9h	DAC1FSC[7:0]							
0Ch	DAC1 FSC MSBs	01h							DAC1FSC[9:8]	
0Dh	AUX DAC1	00h	AUXDAC1[7:0]							
0Eh	AUX DAC1 MSB	00h	AUX1SGN		AUX1DIR				AUXDAC1[9:8]	
0Fh	DAC2 FSC	F9h	DAC2FSC[7:0]							
10h	DAC2 FSC MSBs	01h							DAC2FSC[9:8]	
11h	AUXDAC2	00h	AUXDA2[7:0]							
12h	AUXDAC2 MSB	00h	AUX2SGN		AUX2DIR				AUXDA2[9:8]	
1A	BIST Control	00h	BISTEN		BISTRD		BISTCLR			
1B	BIST Result 1 Low	00h	BISTRES1[7:0]							
1C	BIST Result 1 High	00h	BISTRES1[15:8]							
1D	BIST Result 2 Low	00h	BISTRES2[7:0]							
1E	BIST Result 2 High	00h	BISTRES2[15:8]							
1F	Hardware Version	N/A	VERSION[3:0]				DEVICE[3:0]			

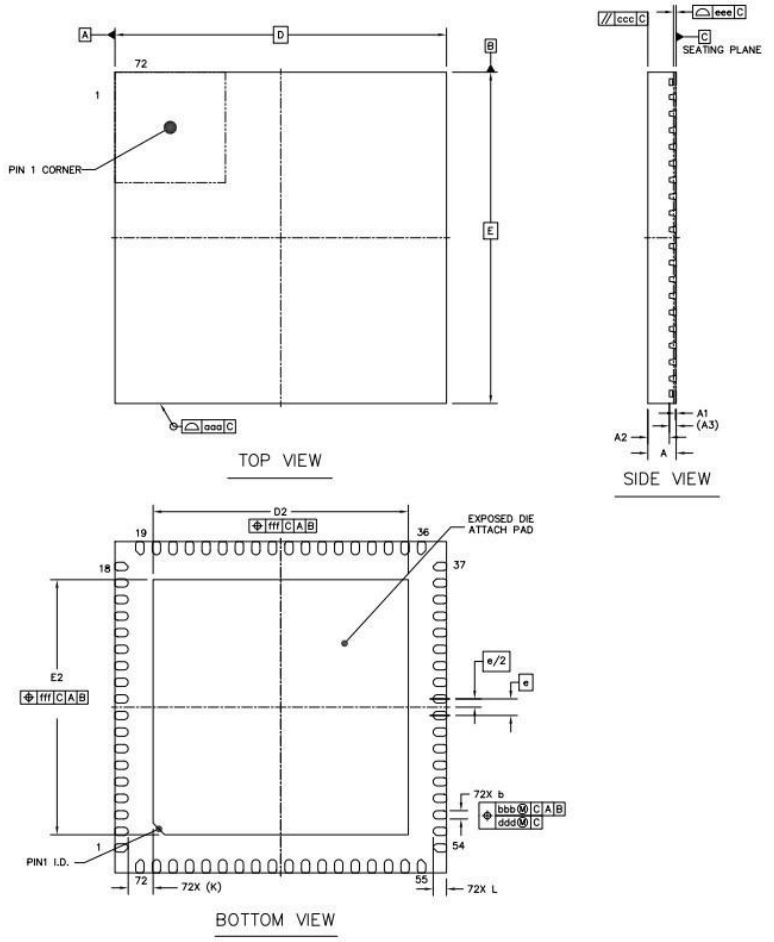
Table 8 Register Description

Register	Address	Bit	Name	Description
SPI Control	0x00	7	SDIODIR	0 = operate SPI in 4-wire mode, SDIO pin operates as an input only 1 = operate SPI in 3-wire mode, SDIO pin operates as a bidirectional input/output line
		6	LSBFIRST	0 = LSBFIRST off 1 = LSBFIRST on Only change LSB/MSB order in single-byte instructions to avoid erratic behavior due to bit order errors.
		5	RESET	0 = execute software reset of SPI and controllers, reload default register values except Register 0x00. 1 = set software reset, write 0 on the next (or any following) cycle to release the reset.
Data Control	0x02	7	DATTYPE	0 = DAC input data is twos complement binary format 1 = DAC input data is unsigned binary format
		4	INVDCO	1 = inverts data clock output signal. Used for adjusting timing of input data.
Power Down	0x03	7	PD_DCO	1 = power down data clock output
		6	PD_INPT	1= power down input.
		5	PD_AUX2	1 = power down AUX2 DAC
		4	PD_AUX1	1 = power down AUX1 DAC
		3	PD_BIAS	1 = power down voltage reference bias circuit
		2	PD_CLK	1 = power down DAC clock input circuit
		1	PD_DAC2	1 = power down DAC2
		0	PD_DAC1	1 = power down DAC1
Setup and Hold	0x04	7:4	SET[3:0]	4-bit value used to determine input data setup timing.
		3:0	HLD[3:0]	4-bit value used to determine input data hold timing
Timing Adjust	0x05	4:0	SAMP_DLY[4:0]	5-bit value used to optimally position input data relative to internal sampling clock.

Version：V1.6
Release Date：2024/02/27

Register	Address	Bit	Name	Description
Mix Mode	0x0A	3:2	DAC1MIX[1:0]	00 = selects Normal Mode. 01 = selects Mix Mode. 10 = selects RZ Mode. 11 = selects RZ Mode.
		1:0	DAC2MIX[1:0]	00 = selects Normal Mode. 01 = selects Mix Mode. 10 = selects RZ Mode. 11 = selects RZ Mode.
DAC1 FSC	0x0B	7:0	DAC1FSC[7:0]	DAC1 full-scale 10-bit adjustment
	0x0C	1:0	DAC1FSC[9:8]	0x03FF = sets full-scale current to the maximum value of 31.66 mA 0x01F9 = sets full-scale current to the nominal value of 20.0 mA 0x0000 = sets full-scale current to the minimum value of 8.64 mA
AUX DAC1	0x0D	7:0	AUXDAC1[7:0]	Auxiliary DAC1 10-bit output current adjustment
	0x0E	1:0	AUXDAC1[9:8]	0x03FF = sets output current to 2.0 mA 0x0200 = sets output current to 1.0 mA 0x0000 = sets output current to 0.0 mA
		7	AUX1SGN	1 = AUX1P output pin is active 0 = AUX1N output pin is active
		6	AUX1DIR	0 = configures AUX1 DAC output to source current 1 = configures AUX1 DAC output to sink current
DAC2 FSC	0x0F	7:0	DAC2FSC[7:0]	DAC2 full-scale 10-bit adjustment
	0x10	1:0	DAC2FSC[9:8]	0x03FF = sets full-scale current to the maximum value of 31.66 mA 0x0200 = sets full-scale current to the nominal value of 20.0 mA 0x0000 = sets full-scale current to the minimum value of 8.64 mA
AUX DAC2	0x11	7:0	AUXDAC2[7:0]	Auxiliary DAC2 10-bit output current adjustment
	0x12	1:0	AUXDAC2[9:8]	0x03FF = sets output current to 2.0 mA 0x0200 = sets output current to 1.0 mA 0x0000 = sets output current to 0.0 mA
		7	AUX2SGN	1 = AUX2P output pin is active 0 = AUX2N output pin is active
		6	AUX2DIR	0 = configures AUX2 DAC output to source current 1 = configures AUX2 DAC output to sink current
BIST Control	0x1A	7	BISTEN	1 = enables and starts built-in self-test.
		6	BISTRD	1 = transfers BIST result registers to SPI for readback.
		5	BISTCLR	1 = reset BIST logic and clear BIST result registers.
BIST Result 1	0x1B	7:0	BISTRES1[15:0]	16-bit result generated by BIST 1.
	0x1C	7:0		
BIST Result 2	0x1D	7:0	BISTRES2[15:0]	16-bit result generated by BIST 2.
	0x1E	7:0		
Hardware Version	0x1F	7:4	VERSION[3:0]	Read only register; indicates the version of the chip
		3:0	DEVICE[3:0]	Read only register; indicates the device type.

OUTLINE DIMENTIONS



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	7.6	7.7	7.8
	Y	E2	7.6	7.7	7.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.75 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Figure 7 QFN-72 10mmx10mm

ORDERING GUIDE

Table 7 Order Information

Part No.	OP Temp	Package
GX9783GDLUB Y	-40~85℃	QFN-72

Note: Packaging can be customized according to customer needs.

DECLARATION

The above information is for reference only, and is intended to assist GXSC (Shenzhen) Technology Co., Ltd customers in their research and development. GXSC (Shenzhen) Technology Co., Ltd reserves the right to change the above information without prior notice due to technological innovation.

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