GX85RS2MC

Ferroelectric random access Memory (FRAM)

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GXSC (Shenzhen) Technology Co., Ltd

Table of Contents

1. Description

GX85RS2MC is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 262,144 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. Unlike SRAM, the chip does not require a battery to hold data.

The memory cells used in the GX85RS2MC can be used for 1E6 read/write operations*1, which is more than FLASH and EEPROM. GX85RS2MC does not take long time to write data like Flash memories or E2PROM, and it takes no wait time.

2. Product Features

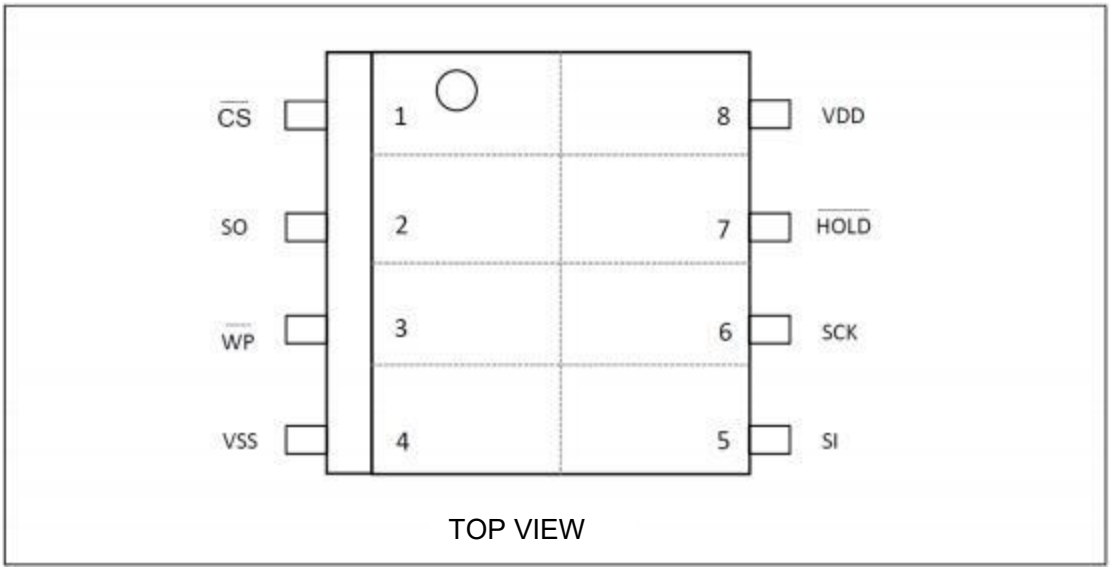
Capacity	2M bit
Interface	SPI interface (Mode 0 and mode 3)
Operating voltage	2.7V to 3.6V
Operating frequency	25MHz
Power consumption	4.8mA (25 MHz)
Low power consumption	9uA (standby)
endurance	106 Read/write (*1 room temperature), 109/ read (room temperature)
Data retention	10 years @ 85C
Fast read features	Support 40MHz fast read command
Operation ambient temperature range	-40℃ to 85℃
Package	8 pin SOP wide-body 208mil package, RoHS compliant

*1: See Instructions for Use

Instructions for use:

- Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.
- recommend programming within the operation temperature range. Working beyond the temperature range for a long time cannot guarantee the data written within the normal temperature.
- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed. Only once reflow soldering guaranteed.

3. Pin Distribution



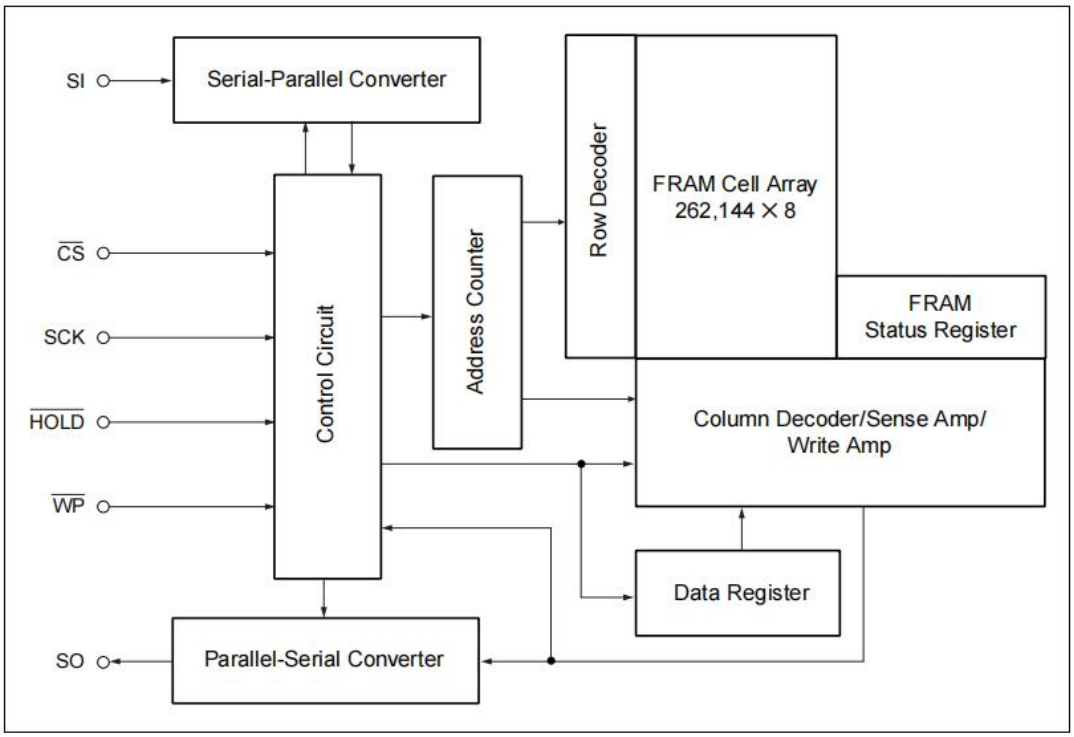
TOP VIEW

4. Pin function description

Pin name	Function description
$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When CS is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When CS is “L” level, device is in select (active) status. CS has to be “L” level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin
SO	Serial Data Output pin
$\overline{WP}$	Write protect pin
VSS	Ground pin
SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data
SCK	Serial Clock pin This is a clock input pin to input/output serial data.

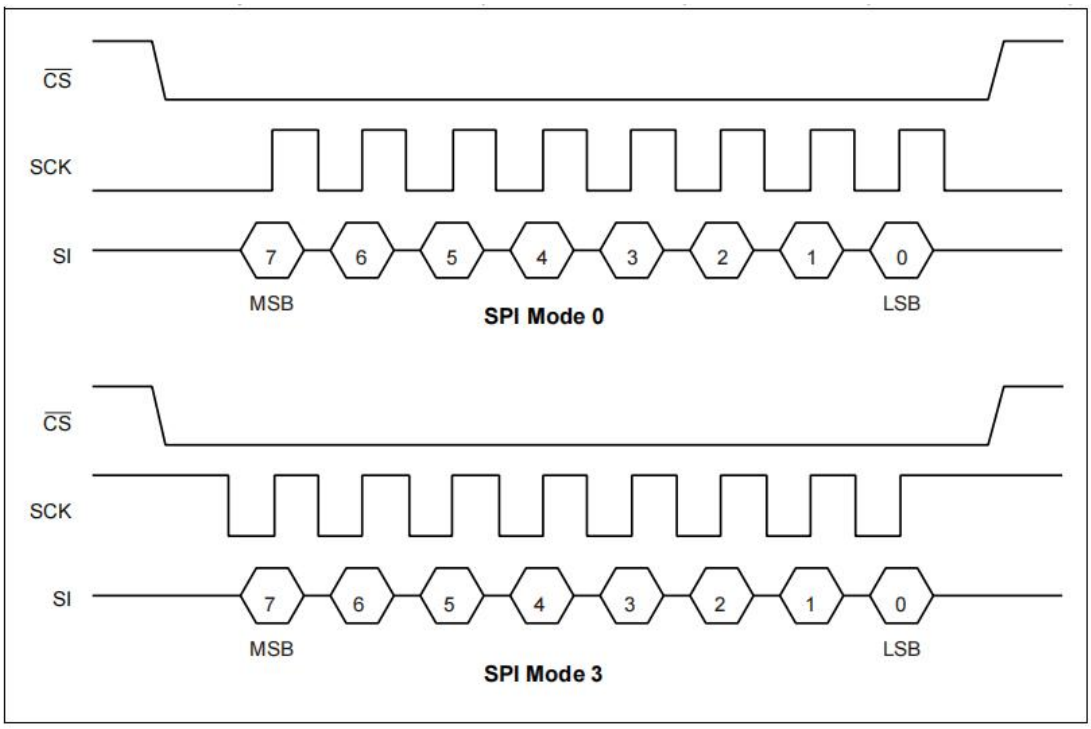
$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When HOLD is “L” level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. While the hold operation, CS has to be retained “L” level.
VDD	Power supply voltage pin

5. Product block diagram



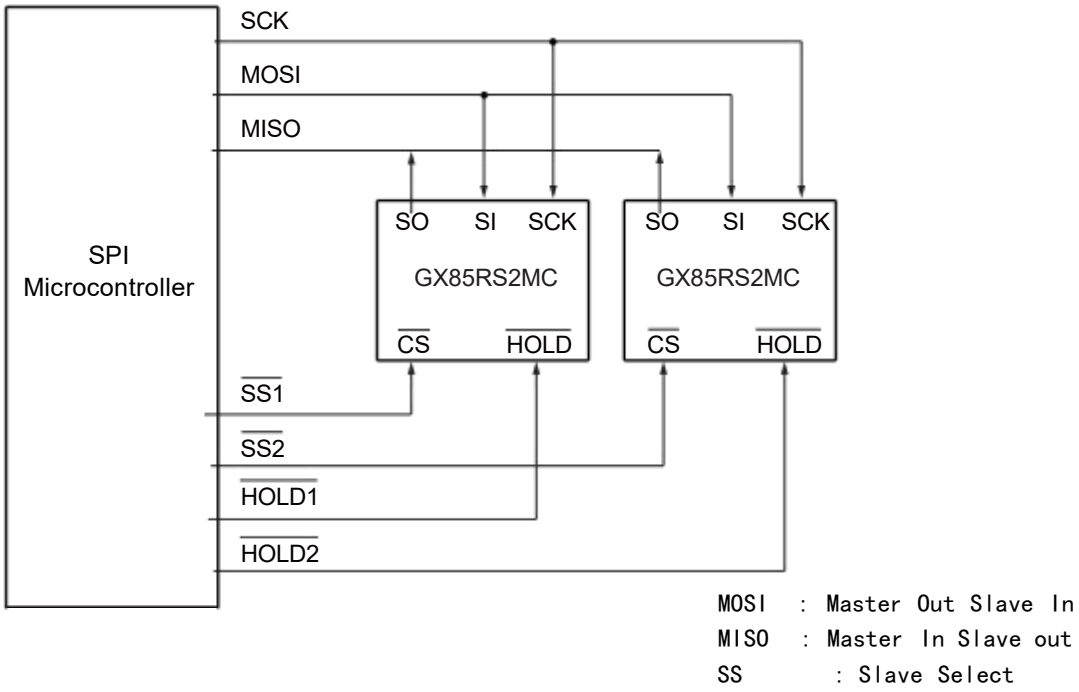
6. Interface mode

GX85RS2MC supports SPI mode 0(CPOL=0,CPHA=0) and SPI mode3(CPOL=1,CPHA=1) communication.

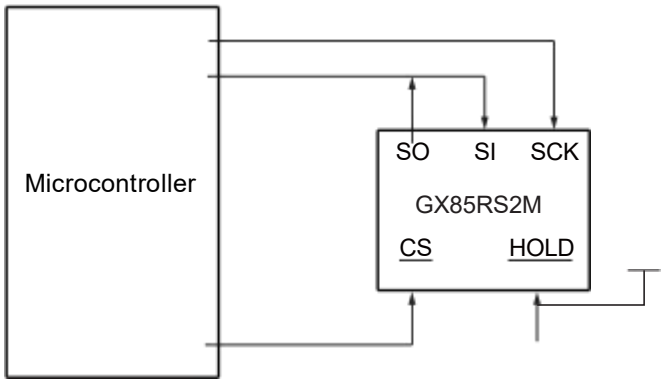


7. Serial peripheral interface

GX85RS2MC works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

8. Status Register

Bit number	Bit name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with WP input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	-	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	

1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. The rising edge of CS after WRSR command recognition. The rising edge of CS after WRITE command recognition.
0	0	This is a bit fixed to "0".

9. OP code

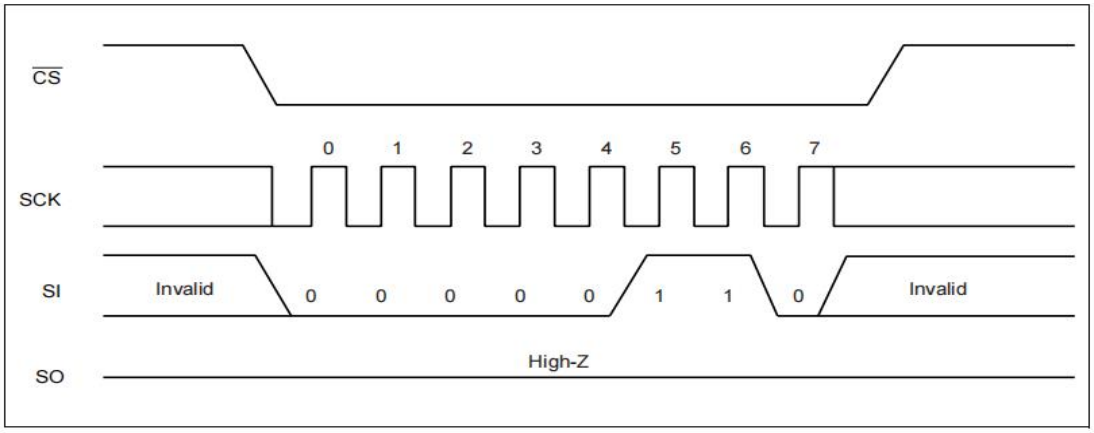
GX85RS2MC accepts 9 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If CS is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110B
WRDI	Reset Write Enable Latch	0000 0100B
READ	Read Memory Code	0000 0011B
WRITE	Write Memory Code	0000 0010B
RDID	Read Device ID	1001 1111B
FSTRD	Fast Read Memory Code	0000 1011B
SLEEP	Sleep Mode	1011 1001B
RDSR	Read status register	0000 0101B
WRSR	Write status register	0000 0001B

10. Command

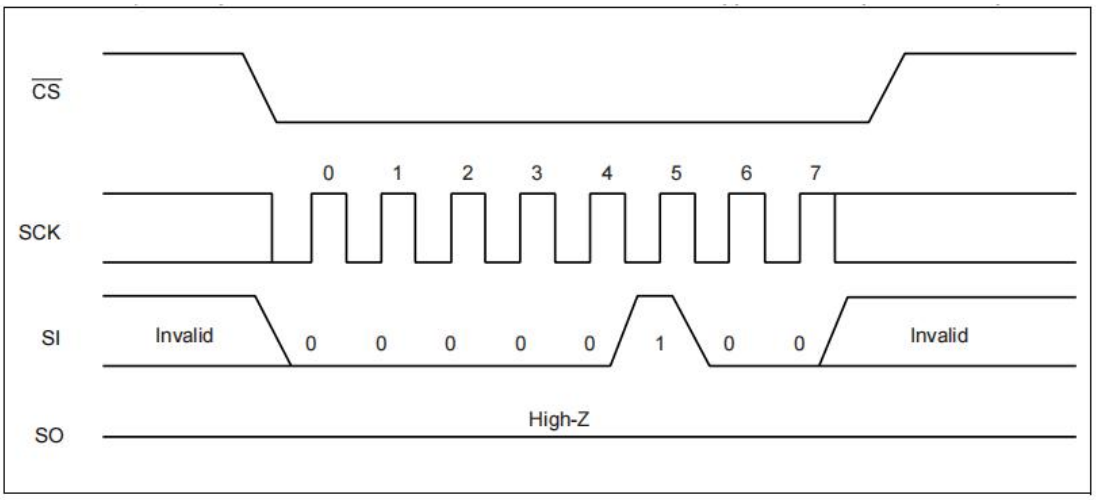
WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) . WREN command is applicable to “Up to 25 MHz operation”



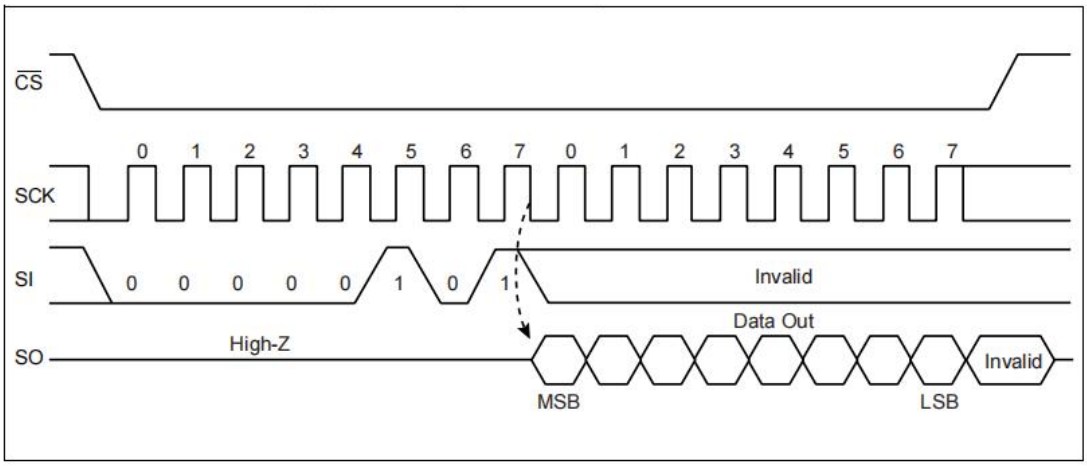
WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset. WRDI command is applicable to “Up to 25 MHz operation”.



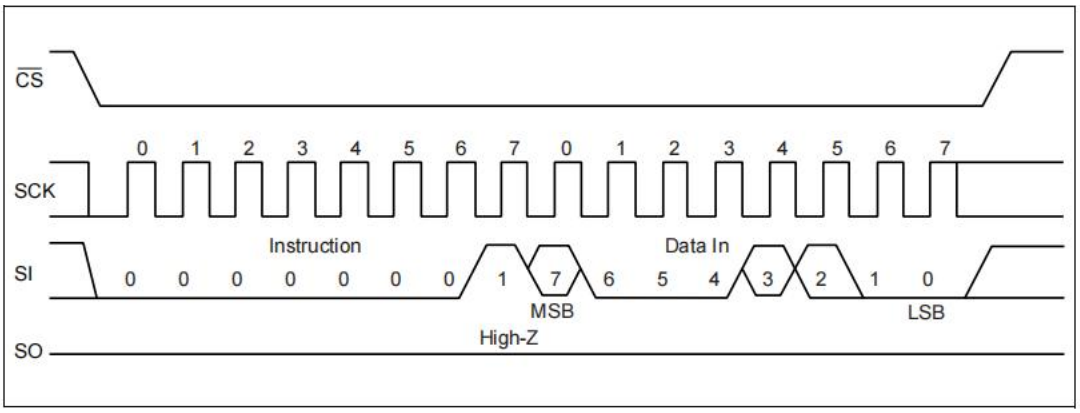
RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of CS. RDSR command is applicable to “Up to 25 MHz operation”.



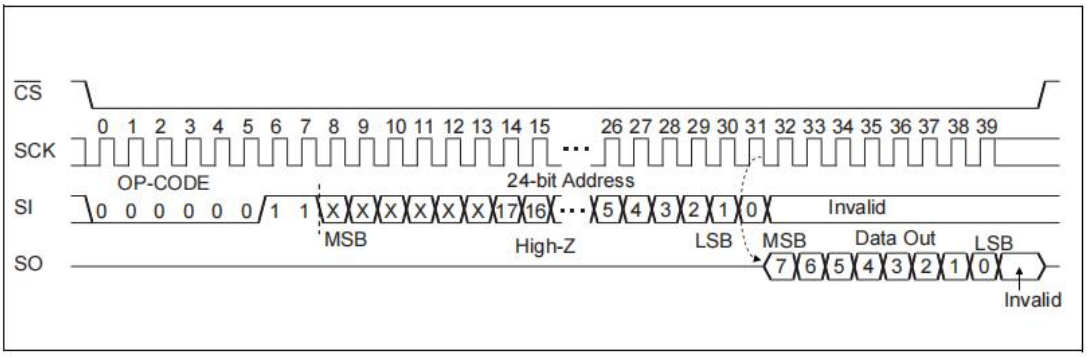
WRSR

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. WP signal level shall be fixed before performing WRSR command, and do not change the WP signal level until the end of command sequence. WRSR command is applicable to “Up to 25 MHz operation”.



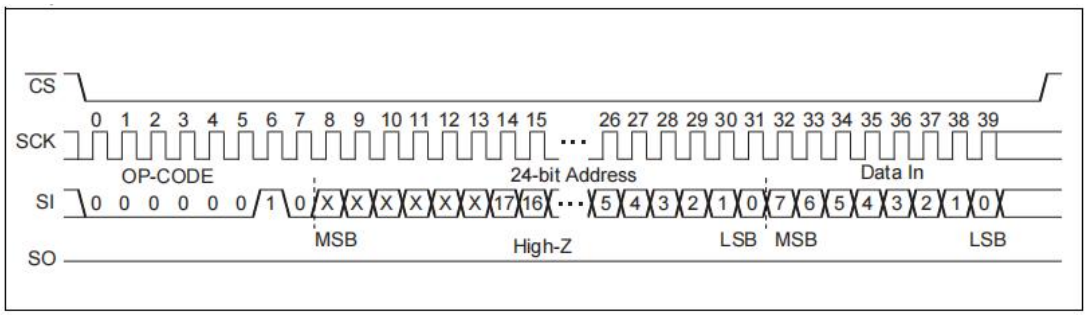
READ

The READ command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When CS is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before CS rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. READ command is applicable to “Up to 25 MHz operation”.



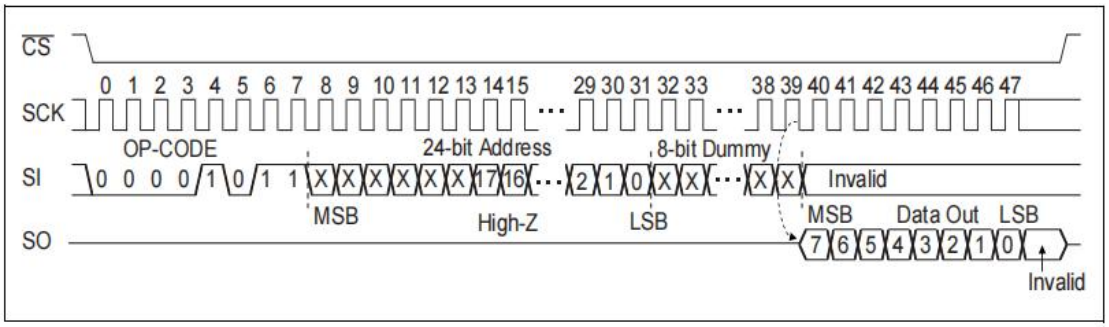
WRITE

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 6-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen CS will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before CS rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely. WRITE command is applicable to “Up to 25 MHz operation”.



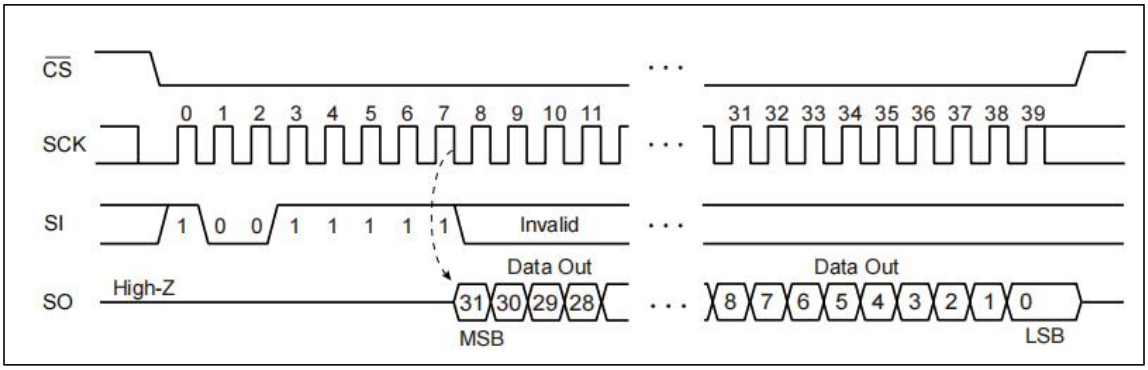
FSTRD

The FSTRD command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When CS is risen, the FSTRD command is completed, but keeps on reading with automatic address incrementwhich is enabled by continuously sending clocks to SCK in unit of 8 cycles before CS rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. FSTRD command is applicable to 40 MHz (2.7 V to 3.6 V) operation.



RDID

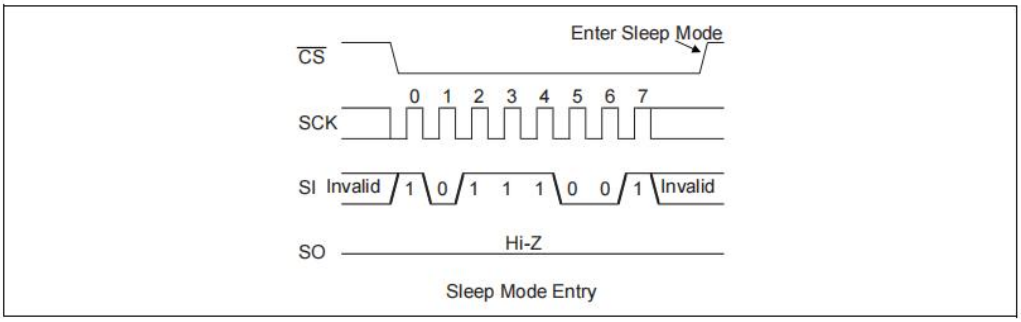
The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until CS is risen. RDID command is applicable to “Up to 25 MHz operation”. Chip ID : Hexadecimal 628C 2400



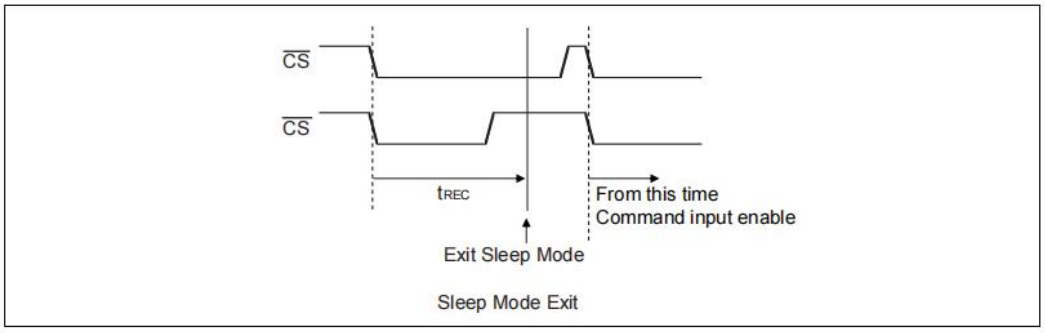
SLEEP

The SLEEP command shifts the LSI to a low power mode called “SLEEP mode”. The transition to the SLEEP mode is carried out at the rising edge of CS after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of CS after operation code in the SLEEP command,this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are ignored and SO changes to a Hi-Z state



Returning to an normal operation from the SLEEP mode is carried out after tREC (1us) time from the falling edge of CS (see the figure below). It is possible to return CS to H level before tREC time. However, it is prohibited to bring down CS to L level again during tREC period



■ Block Protection

The WRITE protection block of the write command is configured by the values of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	30000_H to $3FFFF_H$ (upper 1/4)
1	0	20000_H to $3FFFF_H$ (upper 1/2)
1	1	00000_H to $3FFFF_H$ (all)

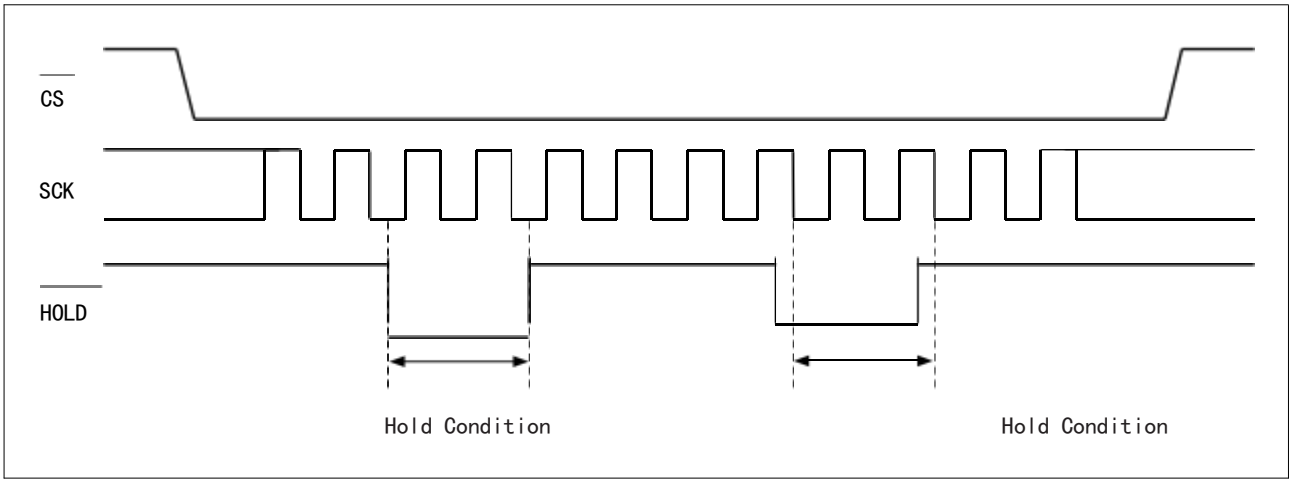
■ Write Protection

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL,WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

11 Hold operation

Hold status is retained without aborting a command if HOLD is “L” level while CS is “L” level. The timing for starting and ending hold status depends on the SCK to be “H” level or “L” level when a HOLD pin input is transited to the hold condition as shown in the diagram below. In case the HOLD pin transited to “L” level when SCK is “L” level, return the HOLD pin to “H” level at SCK being “L” level. In the same manner, in case the HOLD pin transited to “L” level when SCK is “H” level, return the HOLD pin to “H” level at SCK being “H” level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care.
And, SO becomes High-Z while reading command (RDSR, READ). If CS is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



12. Absolute maximum rating

Parameters	Symbols	Rating		Units
		Minimum	Maximum	
Supply voltage	VDD	-0.5	4.0	V
Input voltage	V IN	-0.5	VDD + 0.5	V
Output voltage	VOUT	-0.5	VDD + 0.5	V
Operation ambient temperature	TA	-40	85	℃
Storage temperature	Tstg	-40	125	℃

*1: The above parameter values are based on VSS = 0V.

*2: The above storage temperature is the ambient temperature that the device can store before writing data. After the device writes data, please refer to the working ambient temperature

< Warning > Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.

Do not exceed any of these ratings.

13. Recommended working conditions

Parameters	Symbols	Numerical value			Units
		Minimum	Typical value	Maximum value	
Supply voltage	VDD	2.7	3.3	3.6	V
Operation ambient temperature	TA	- 40		+ 85	℃

*1: The above parameter values are based on VSS = 0V

*2: Only applicable to the ambient temperature of the chip during operation. It can be understood that this temperature is almost the same as the temperature of the chip surface.

< Warning > In order to ensure the normal operation of the semiconductor device, it must be used in the recommended operating environment or conditions.

All electrical characteristics of the device can be guaranteed when operating in the recommended environment or condition. Be sure to use the semiconductor device within the recommended operating environment or condition. If used outside this range, it may affect the reliability of the device and cause failure.

The Company does not guarantee any scope of use, operating conditions or logical combinations not recorded in this data sheet. If the user wishes to use the device outside the conditions listed, it is important to contact the sales representative in advance.

14. Electrical characteristics

■ Dc characteristics

(within recommended operating conditions)

Parameters	Symbols	Conditions	Numerical value			Units
			Minimum	Typical value	Maximum value	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	–	–	1	μA
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	–	–	1	μA
Working power supply current	I_{DD}	SCK = 25MHz SO = open	–	4.8	5.6	mA
Standby current	I_{SB}	SCK = SI = $\overline{CS}$ = V_{DD}	–	9	12	μA
Sleep current	I_{ZZ}	$\overline{CS}$ = V_{DD} All other inputs V_{SS} or V_{DD}	–	3	4	μA
Input high voltage	V_{IH}	V_{DD} = 2.7V to 3.6V	V_{DD} * 0.7	–	V_{DD} + 0.3	V
Input low voltage	V_{IL}	V_{DD} = 2.7V to 3.6V	0.5	–	V_{DD} * 0.3	V
Output high voltage	V_{OH}	I_{OH} = -2mA	V_{DD} - 0.5	–	V_{DD}	V
Output low voltage	V_{OL}	I_{OL} = 2mA	V_{SS}	–	0.4	V
CS Pull up resistors	R_P	—	18	33	80	kΩ

■ Communication characteristics

Parameter	sym bol	Numerical		unit
		Min	Max	
Clock frequency (commands other than FSTRD)	f_{CK}	0	25	MHz
Clock frequency (FSTRD command)	f_{CK}	0	40	MHz
Clock high level time	t_{CH}	11	—	ns
Clock low time	t_{CL}	11	—	ns
Chip select setup time	t_{CSU}	10	—	ns
Chip select hold time	t_{CSH}	10	—	ns
Output disabled time	t_{OD}	—	12	ns
Output data valid time	t_{ODV}	—	9	ns
Output hold time	t_{OH}	0	—	ns
Deselect time	t_{D}	40	—	ns
Data on rise time	t_{R}	—	50	ns
Data drop time	t_{F}	—	50	ns
Data setup time	t_{SU}	5	—	ns
Data retention time	t_{H}	5	—	ns
$\overline{\text{HOLD}}$ Set time	t_{HS}	10	—	ns
$\overline{\text{HOLD}}$ Hold time	t_{HH}	10	—	ns
$\overline{\text{HOLD}}$ Output float time	t_{HZ}	—	20	ns
$\overline{\text{HOLD}}$ Output activation time	t_{LZ}	—	20	ns
SLEEP exit time	t_{REC}	1	—	μs

Communication Test conditions

Supply voltage : 2.7V to 3.6V

Operating temperature range : -40℃ to +85℃

Input voltage range :$V_{DD} * 0.7 \le V_{IH} \le V_{DD}$，$0 \le V_{IL} \le V_{DD} * 0.3$

Input rising time : 5ns

input falling time : 5ns

input judge level : $V_{DD} * 0.5$

Output judge level : $V_{DD} * 0.5$

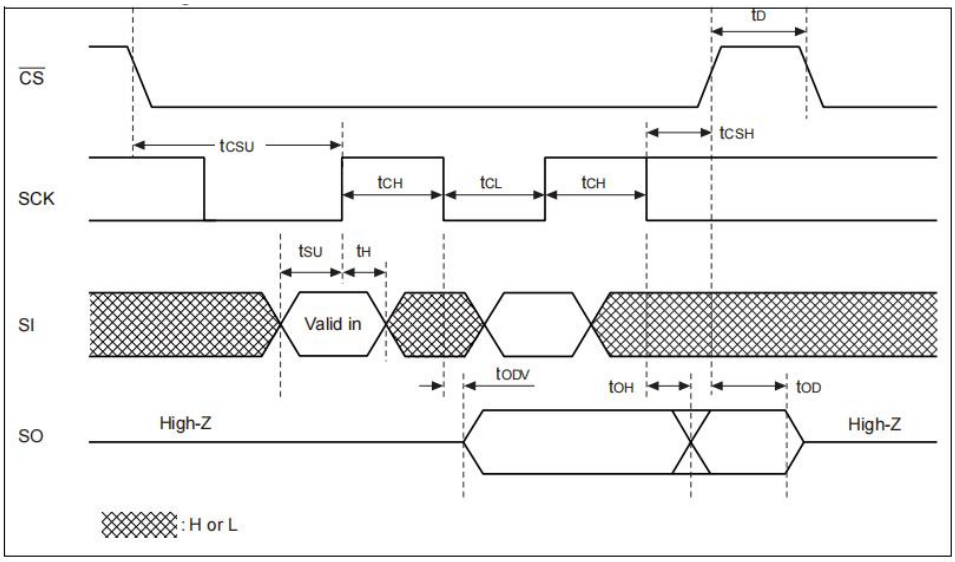
Output load capacitance: 30pF

■ Pin capacitance

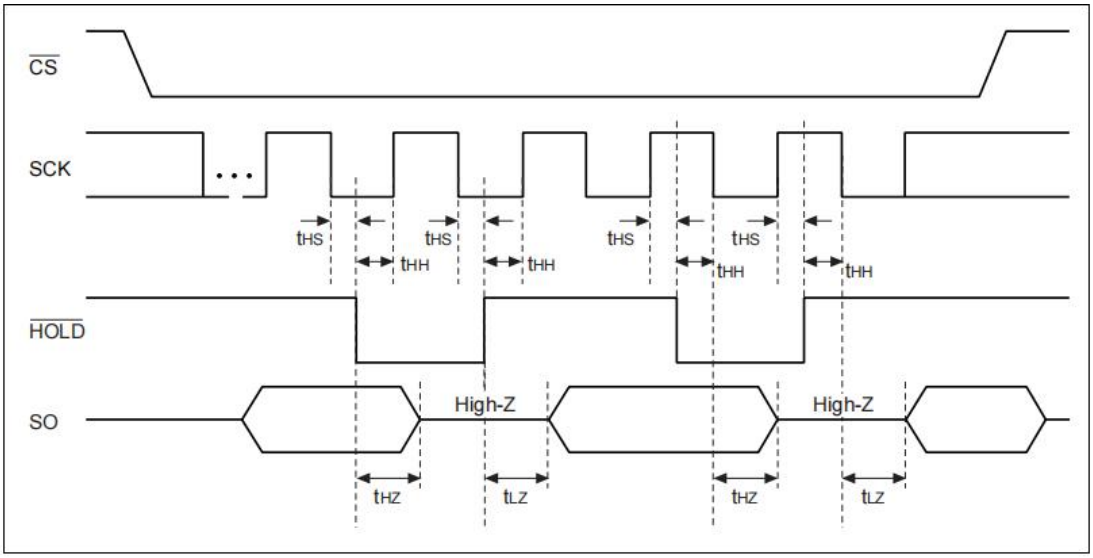
Parameters	Symbol s	Conditions	Numerical value		Units
			Minimum	Maximum	
Output capacitance	C_0	$V_{DD} = V_{IN} = V_{OUT} = 0V$, $f = 1MHz$, $T_A = +25℃$	–	10	pF
Input capacitor	C_I		–	10	pF

15. Timing chart

Serial Data Timing



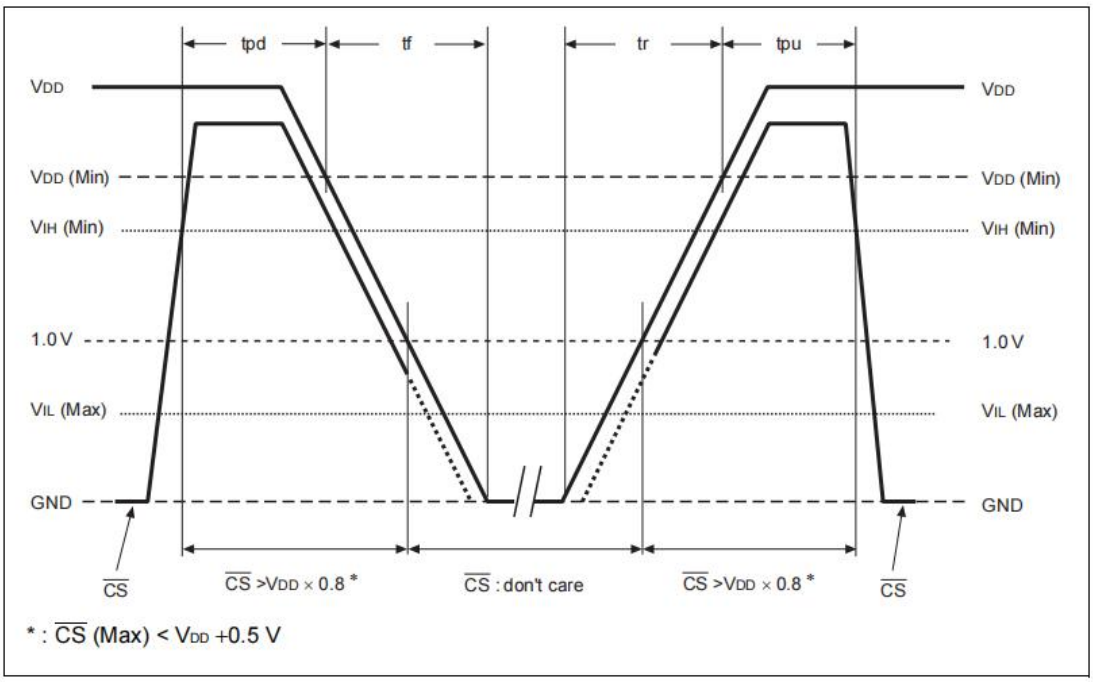
Hold timing



16. Power on/off timing

Parameters	Symbols	Numerical value		Units
		Minimum	Maximum	
CS level hold time at power OFF	t_{pd}	200	–	ns
CS level hold time at power ON	t_{pu}	50	–	μs
Power supply falling time	t_f	20	–	μs
Power supply rising time	t_r	20	–	μs

Note: Storage of data is not guaranteed if the device cannot operate within specific conditions of read cycle, write cycle, or power on/off timing.



17.FRAM features

Parameters	Minimum value	Maximum	Units	Remarks
Read and write endurance*1	1E6	—	Times/byte	operation ambient temperature T_A = -40℃
	1E6	—	Times/byte	operation ambient temperature T_A = +25℃
	1E5	—	Times/byte	operation ambient temperature T_A = +85℃
Data retention*2	—	—	year	operation ambient temperature T_A = -40℃
	—	—	year	operation ambient temperature T_A = +25℃
	10	—	year	operation ambient temperature T_A = +85℃

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory

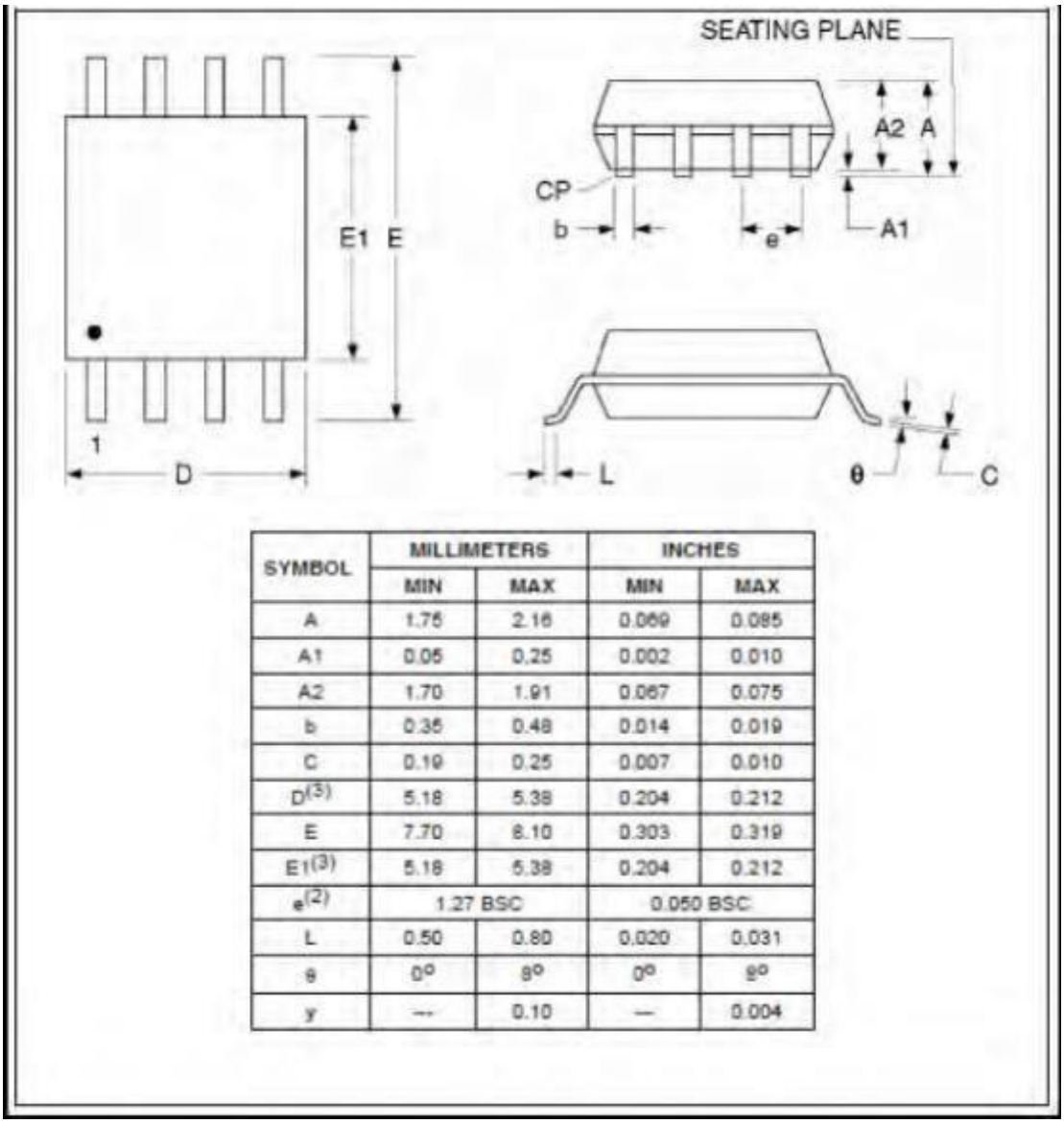
operates with destructive readout mechanism; See "Instructions for Use" for details.

*2: Data retention years indicate the data retention time after the first read and write operation after delivery from the factory. These retention times are converted values based on reliability assessment results; See the Instructions for Use for details

18 ESD and latch

Test	Numerical value
ESD HBM (mannequin) JS-001 compliant	⩾ |2000 V|
ESD CDM (Charging device model) JS-002 compliant	⩾ |1000 V|
Latch-up Comply with JESD78	⩾ |300 mA|

19. Package size 8-Pin SOIC 208-mil



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D(3)	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1(3)	5.18	5.38	0.204	0.212
e(2)	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	—	0.10	—	0.004

联系我们:
联系人:JESSE
EMAIL:service_jesseli@gxschip.com
WECHAT:f40044269
FACEBOOK:GXSC
VK:@id836505054